

EE 330

Lecture 39

Digital Circuits

Sizing of Devices for Logic Circuits

Ratio Logic

Other MOS Logic Families

Propagation Delay – basic characterization

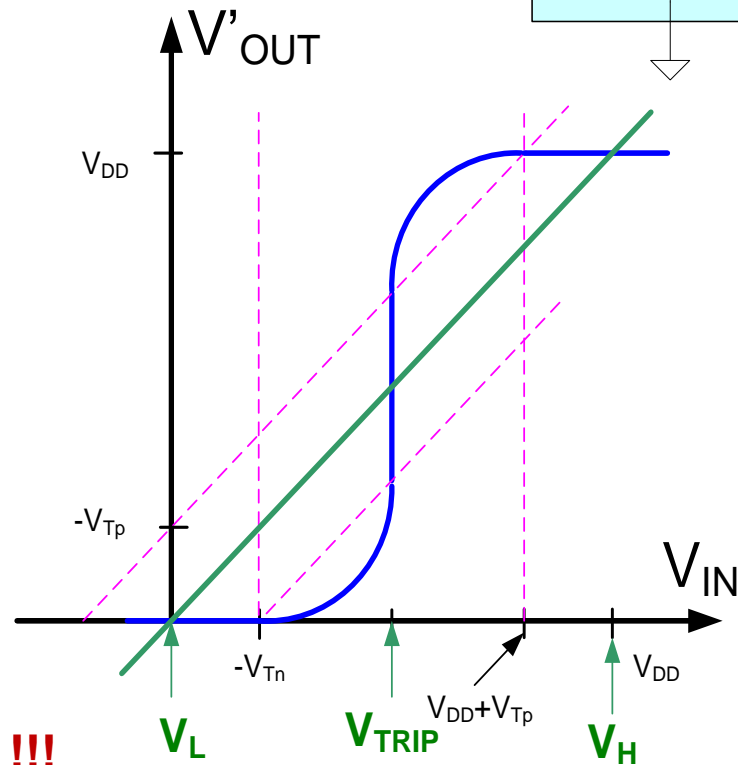
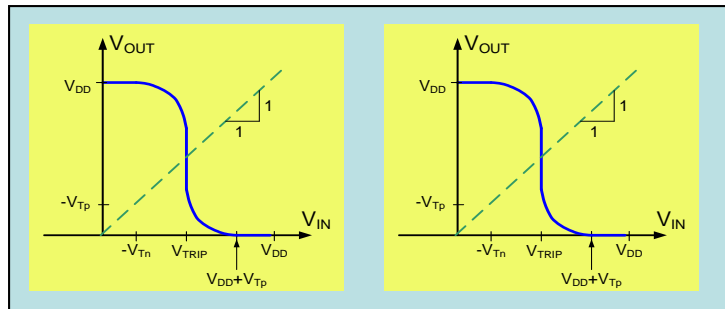
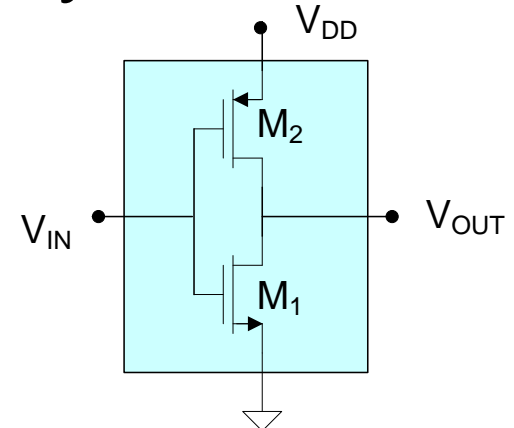
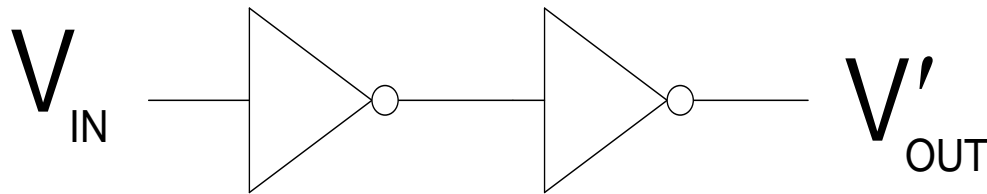
Device Sizing (Inverter and multiple-input gates)

Fall 2023 Exam Schedule

Exam 1	Friday Sept 22	
Exam 2	Friday Oct 20	
Exam 3	Friday Nov. 17	
Final	Monday Dec 11	12:00 – 2:00 p.m.

Review from last lecture

Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family



$$V_H = V_{DD} \text{ and } V_L = 0$$

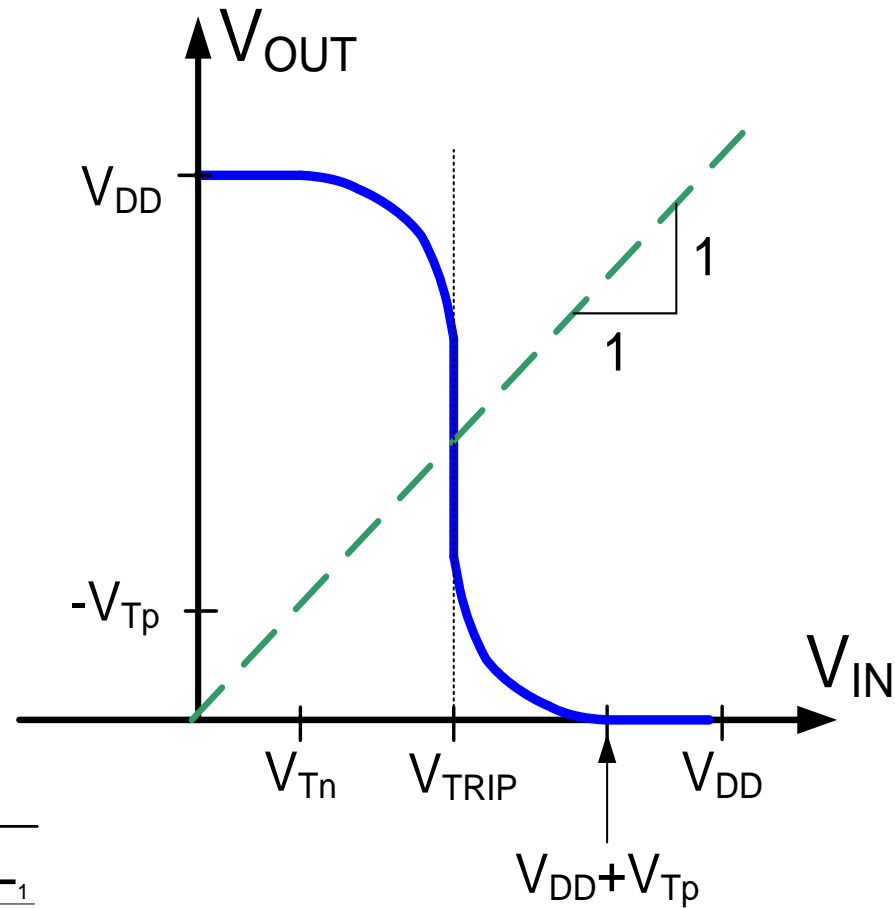
Note this is independent of device sizing for THIS logic family !!

Device sizing does not affect V_H and V_L !!!

Review from last lecture

Transfer characteristics of the static CMOS inverter

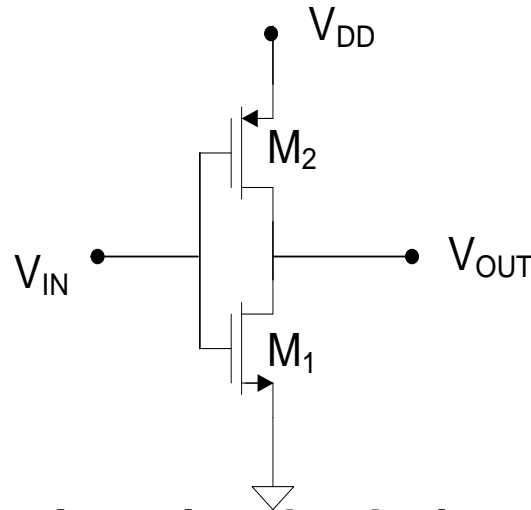
(Neglect λ effects)



From Case 3 analysis:

$$V_{IN} = \frac{(V_{Tn}) + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} \frac{L_1}{L_2}}}$$

Sizing of the Basic CMOS Inverter



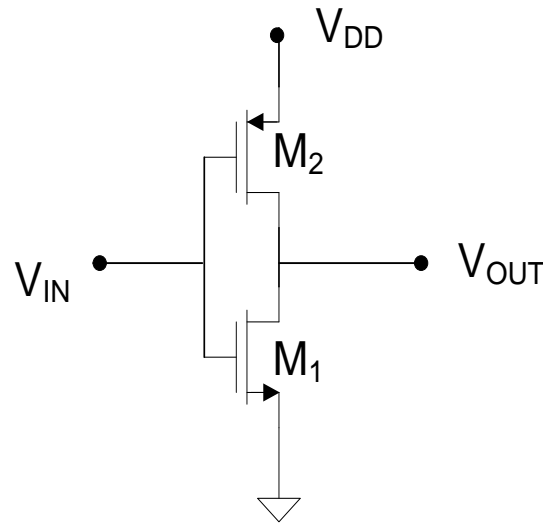
Most logic families require using the device sizing variables to determine acceptable V_H and V_L values

The characteristic that device sizes do not need to be used to establish V_H and V_L logic levels is a major advantage of this type of logic !!

How should M_1 and M_2 be sized?

How many degrees of freedom are there in the design of the inverter?

How should M_1 and M_2 be sized?



How many degrees of freedom are there in the design of the inverter?

$$\{ W_1, W_2, L_1, L_2 \}$$

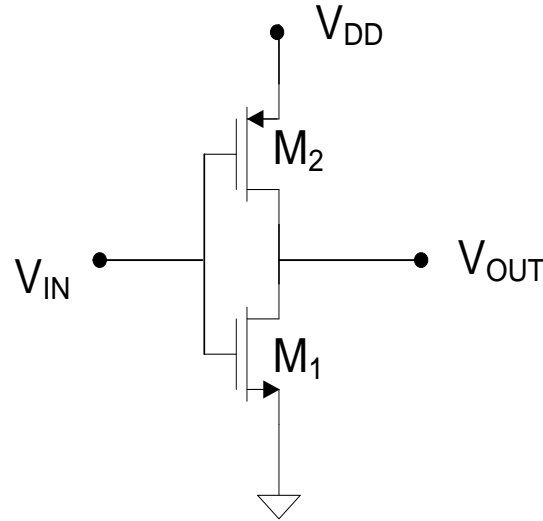
4 degrees of freedom

But in basic device model and in most performance metrics, W_1/L_1 and W_2/L_2 appear as ratios

$$\{ W_1/L_1, W_2/L_2 \}$$

effectively 2 degrees of freedom

How should M_1 and M_2 be sized?



$\{ W_1, W_2, L_1, L_2 \}$ 4 degrees of freedom Usually pick $L_1=L_2=L_{min}$

That leaves $\{ W_1, W_2 \}$ effectively 2 degrees of freedom

How are W_1 and W_2 chosen?

Depends upon what performance parameters are most important for a given application!

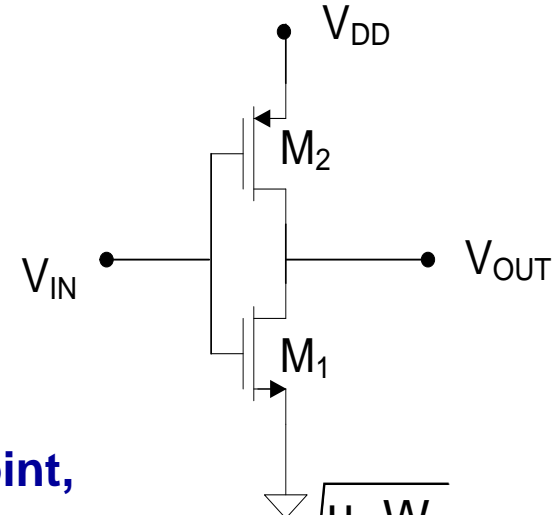
How should M_1 and M_2 be sized?

Pick $L_1=L_2=L_{\min}$

One popular sizing strategy:

1. Pick $W_1=W_{\min}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for V_{TRIP}

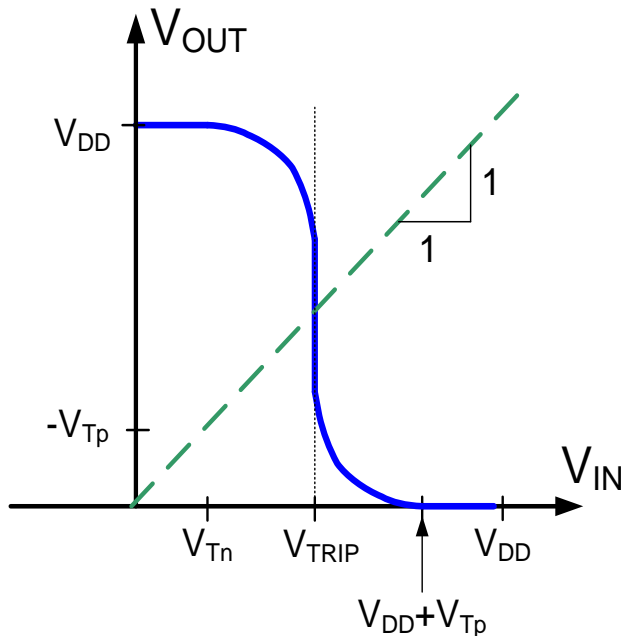


Thus, at the trip point,

$$V_{\text{OUT}} = V_{\text{IN}} = V_{\text{TRIP}} = \frac{(V_{\text{Tn}}) + (V_{\text{DD}} + V_{\text{Tp}}) \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1}}}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1}}}$$

If $V_{\text{Tn}} = -V_{\text{Tp}}$

$$\frac{V_{\text{DD}}}{2} = \frac{(V_{\text{Tn}}) + (V_{\text{DD}} - V_{\text{Tn}}) \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1}}}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1}}}$$



How should M_1 and M_2 be sized?

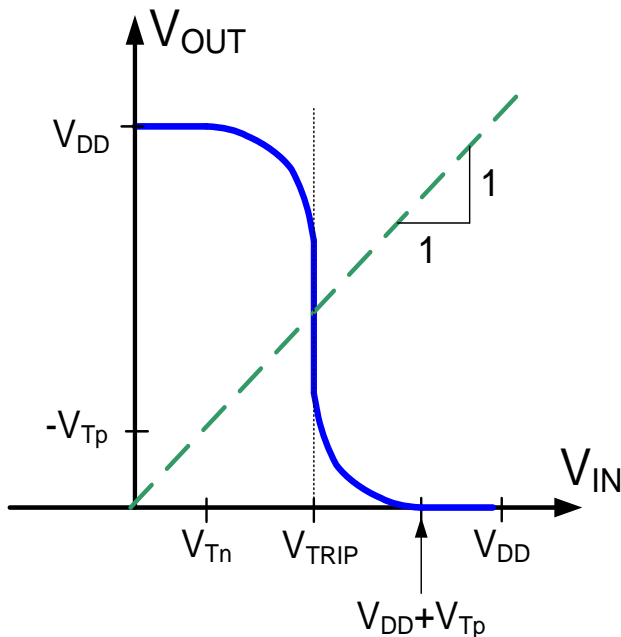
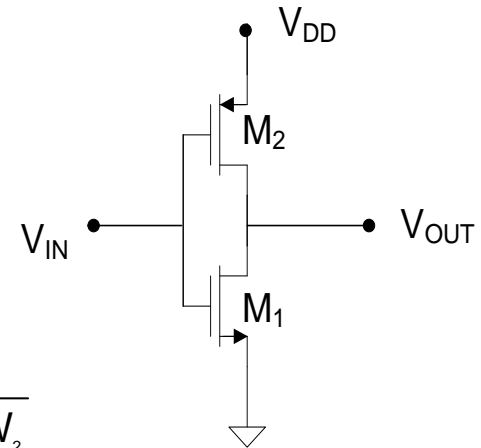
Pick $L_1=L_2=L_{\min}$

One popular sizing strategy:

1. Pick $W_1=W_{\min}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for V_{TRIP}

(solution continued)



$$\frac{V_{DD}}{2} = \frac{(V_{Tn}) + (V_{DD} - V_{Tn}) \sqrt{\frac{\mu_p W_2}{\mu_n W_1}}}{1 + \sqrt{\frac{\mu_p W_2}{\mu_n W_1}}}$$

solving for $\sqrt{\frac{\mu_p W_2}{\mu_n W_1}}$ we obtain

$$\sqrt{\frac{\mu_p W_2}{\mu_n W_1}} = \frac{V_{Tn} - \frac{V_{DD}}{2}}{-\frac{V_{DD}}{2} + V_{Tn}} = 1$$

thus

$$\frac{W_2}{W_1} = \frac{\mu_n}{\mu_p} \Rightarrow W_2 = \frac{\mu_n}{\mu_p} W_{\min} \approx 3W_{\min}$$

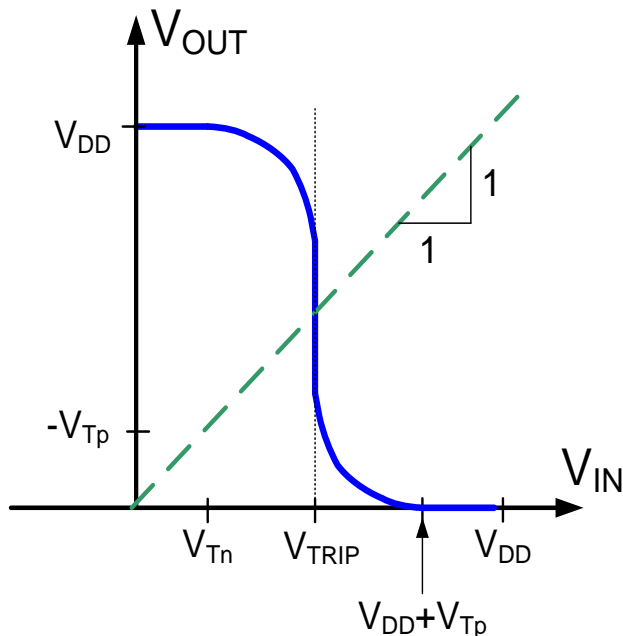
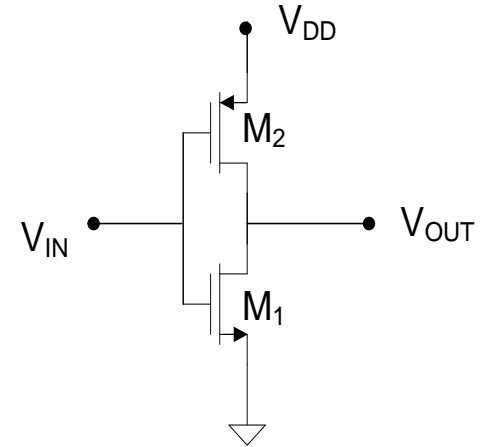
How should M_1 and M_2 be sized?

Pick $L_1=L_2=L_{\min}$

One popular sizing strategy:

1. Pick $W_1=W_{\min}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for V_{TRIP}



Summary: $V_{TRIP} = \frac{V_{DD}}{2}$ sizing strategy

$$L_1=L_2=L_{\min}$$

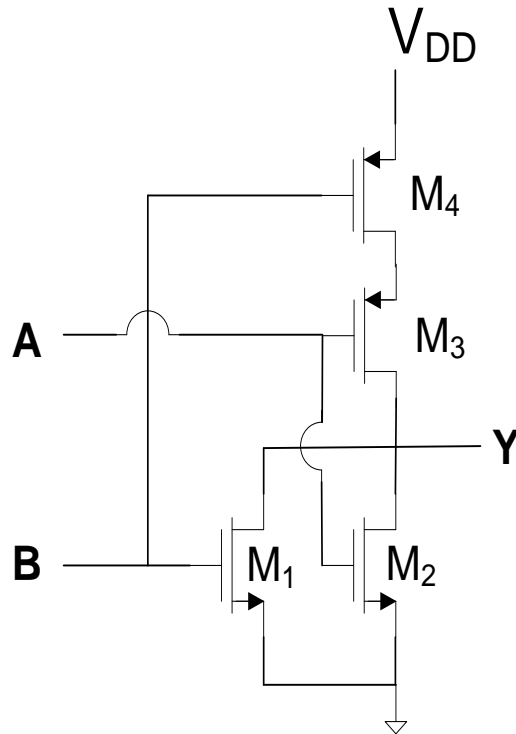
$$W_1=W_{\min}$$

$$W_2 = \frac{\mu_n}{\mu_p} W_{\min} \approx 3W_{\min}$$

(dependent upon assumption $V_{Tp} = -V_{Tn}$)

Other sizing strategies will be discussed later !

Extension of Basic CMOS Inverter to Multiple-Input Gates



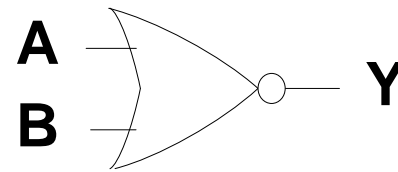
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

Performs as a 2-input NOR Gate

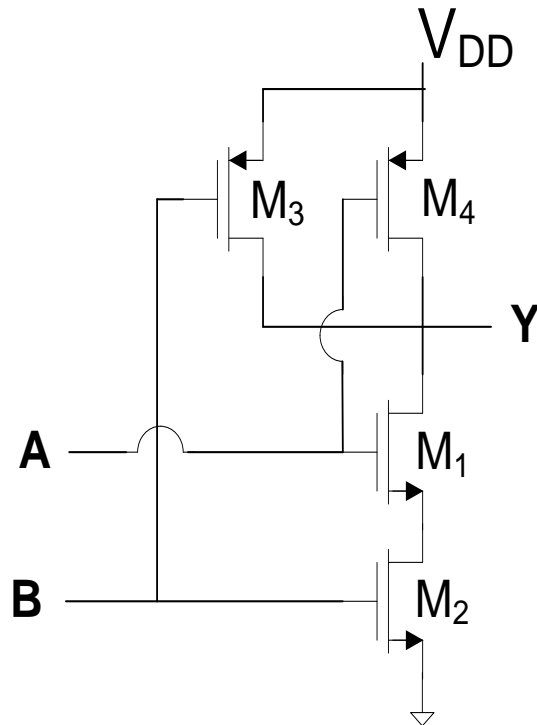
Can be easily extended to an n-input NOR Gate

$V_H = V_{DD}$ and $V_L = 0$ (inherited from inverter analysis)



analysis not shown here but straightforward and consistent with claim that performance of gates in logic family determined by those of basic inverter

Extension of Basic CMOS Inverter to Multiple-Input Gates



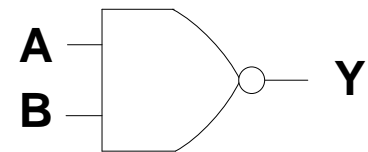
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

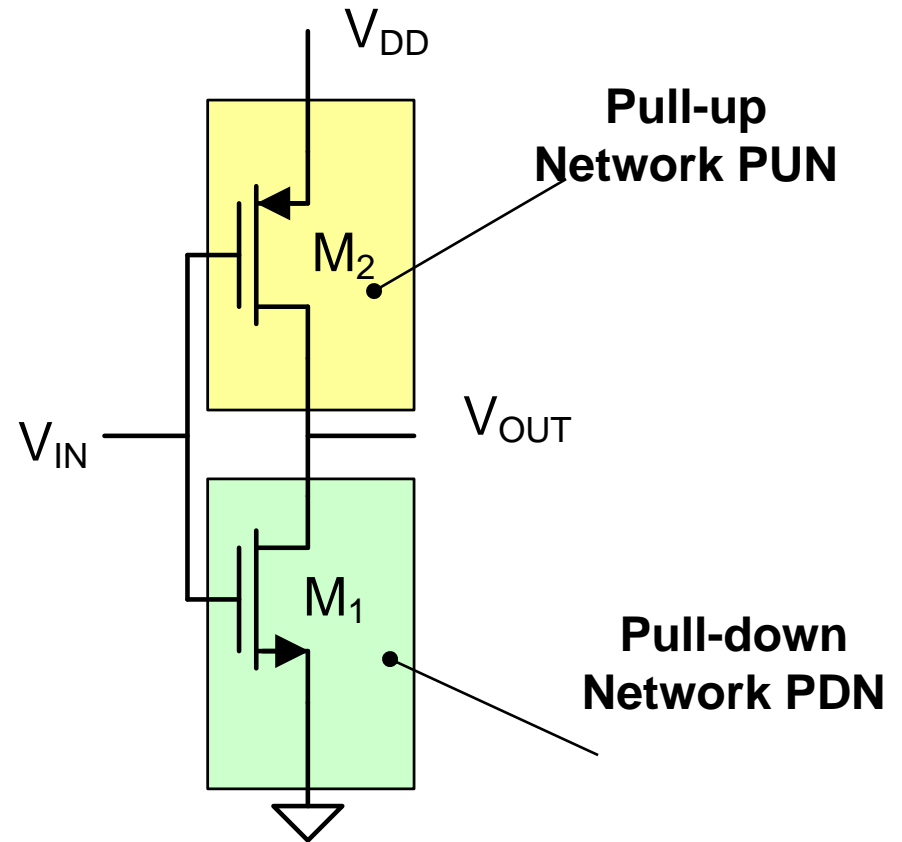
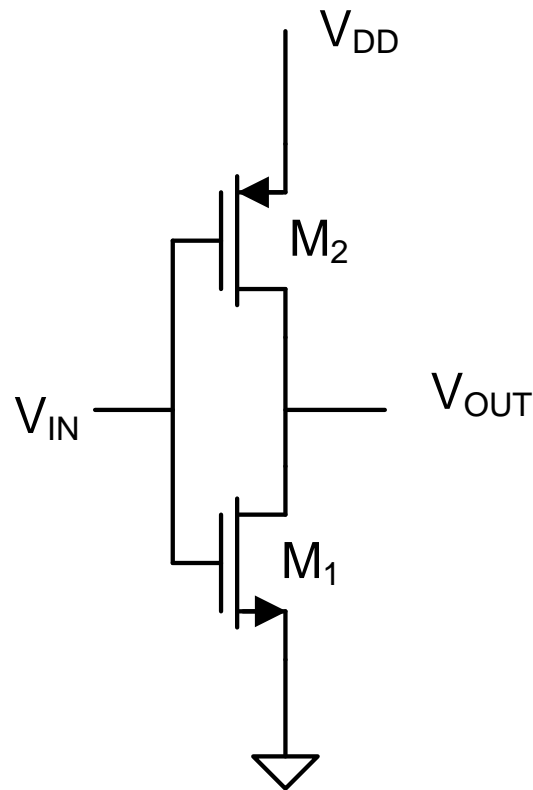
Performs as a 2-input NAND Gate

Can be easily extended to an n-input NAND Gate

$V_H = V_{DD}$ and $V_L = 0$ (inherited from inverter analysis)



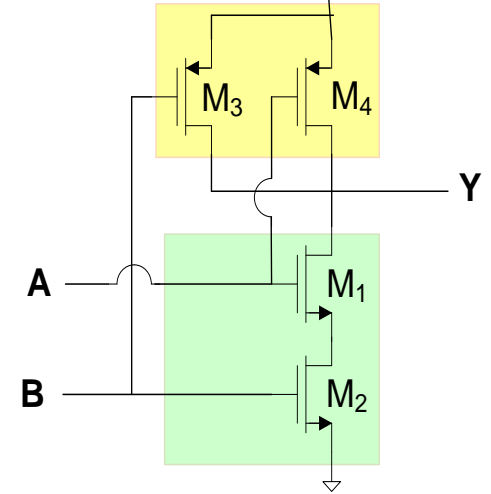
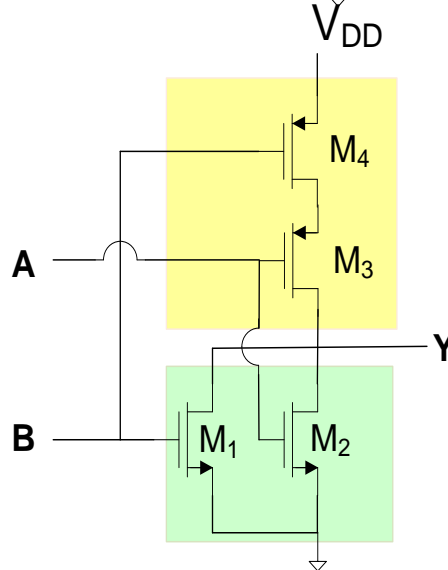
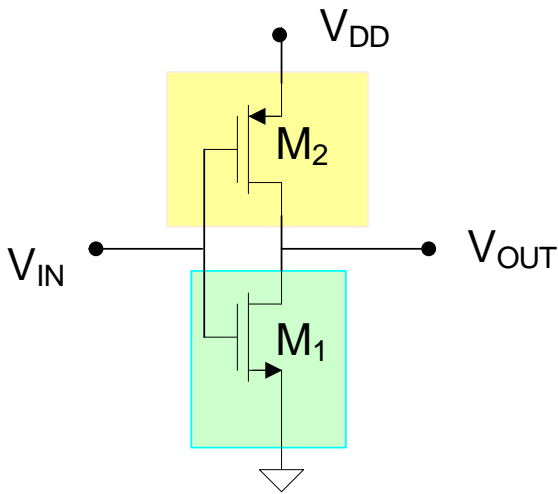
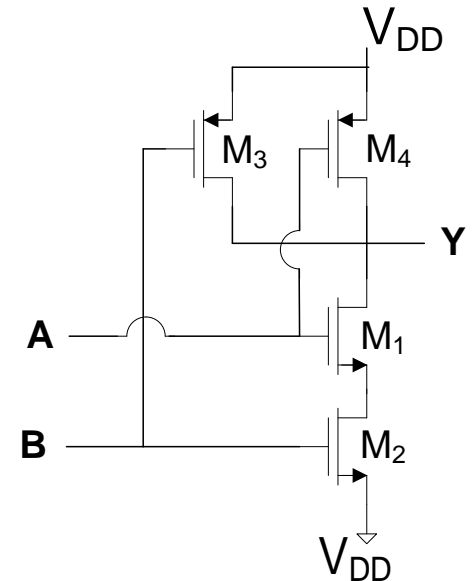
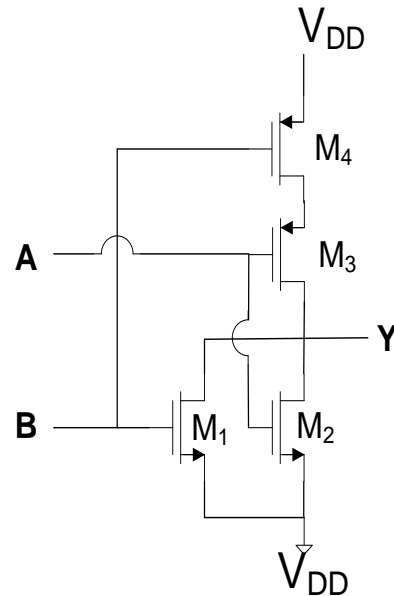
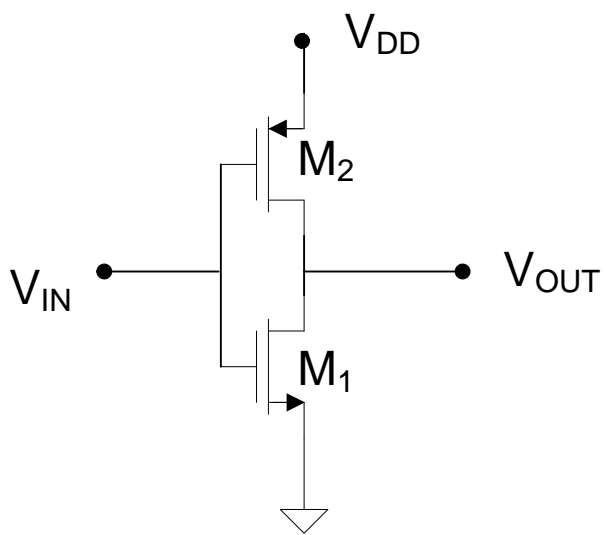
Static CMOS Logic Family



Observe PUN is p-channel, PDN is n-channel

$V_H = V_{DD}$ and $V_L = 0$ (inherited from inverter analysis)

Static CMOS Logic Family



n-channel PDN and p-channel PUN

$V_H = V_{DD}$, $V_L = 0V$ (same as for inverter!)

Digital Circuit Design

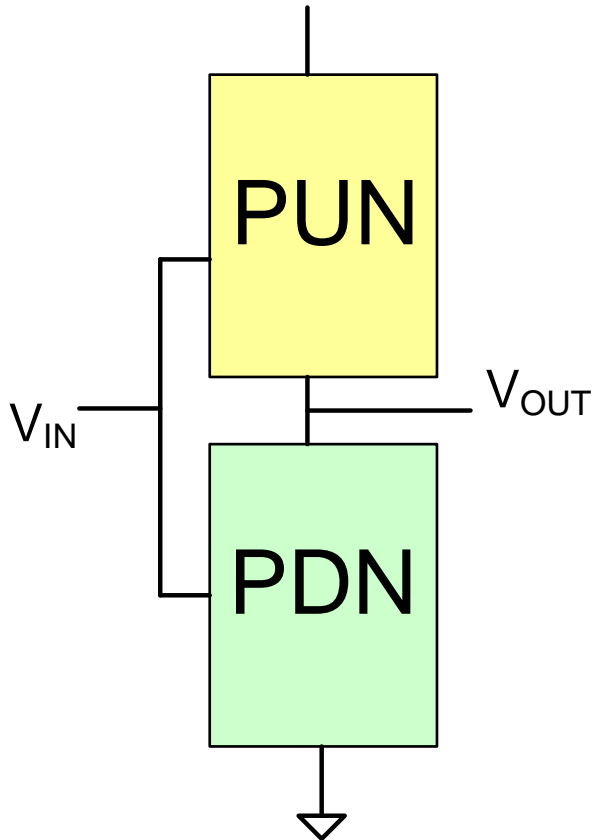
- Hierarchical Design
 - Basic Logic Gates
 - Properties of Logic Families
 - Characterization of CMOS Inverter
 - Static CMOS Logic Gates
 - Ratio Logic
 - Propagation Delay
 - Simple analytical models
 - FI/OD
 - Logical Effort
 - Elmore Delay
 - Sizing of Gates
 - The Reference Inverter
-

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

→ **done**

→ **partial**

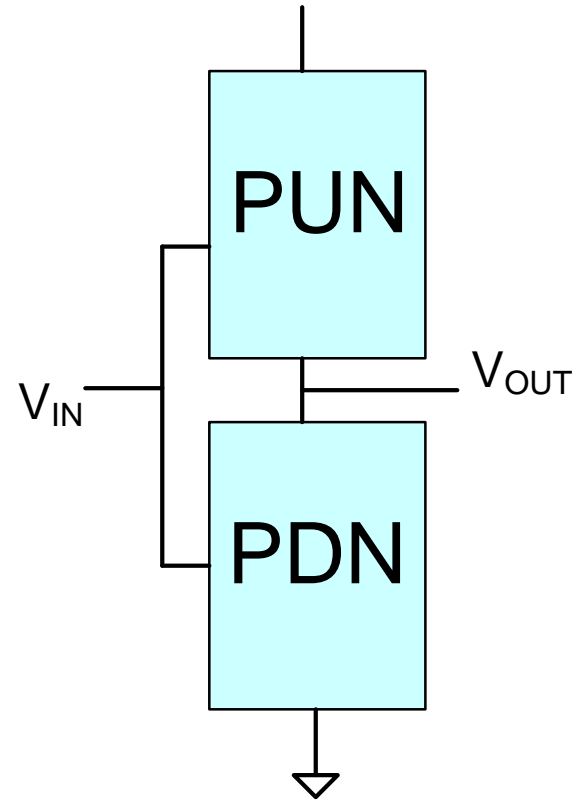
General Logic Family



Compound Gate in CMOS Process

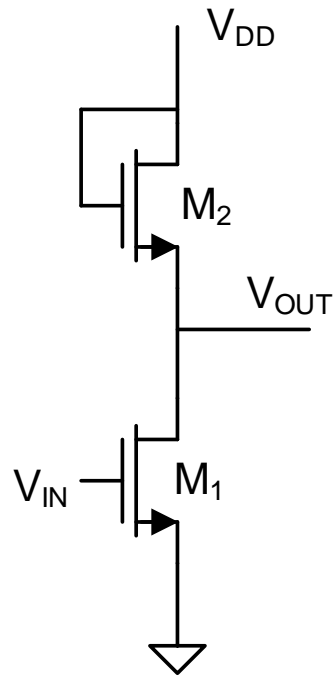
p-channel PUN
n-channel PDN

$V_H = V_{DD}$, $V_L = 0V$ (same as for inverter!)

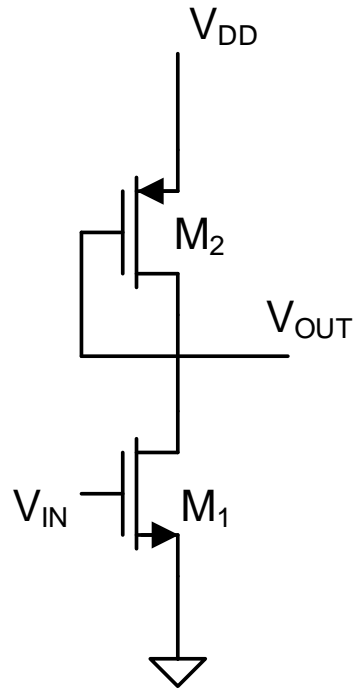


**Arbitrary PUN
and PDN**

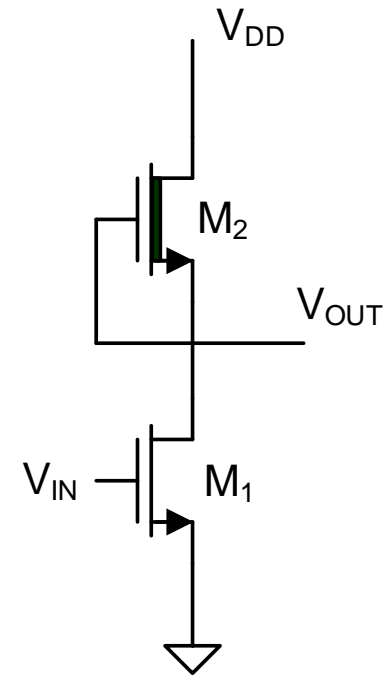
Other MOS Logic Families



Enhancement Load
NMOS

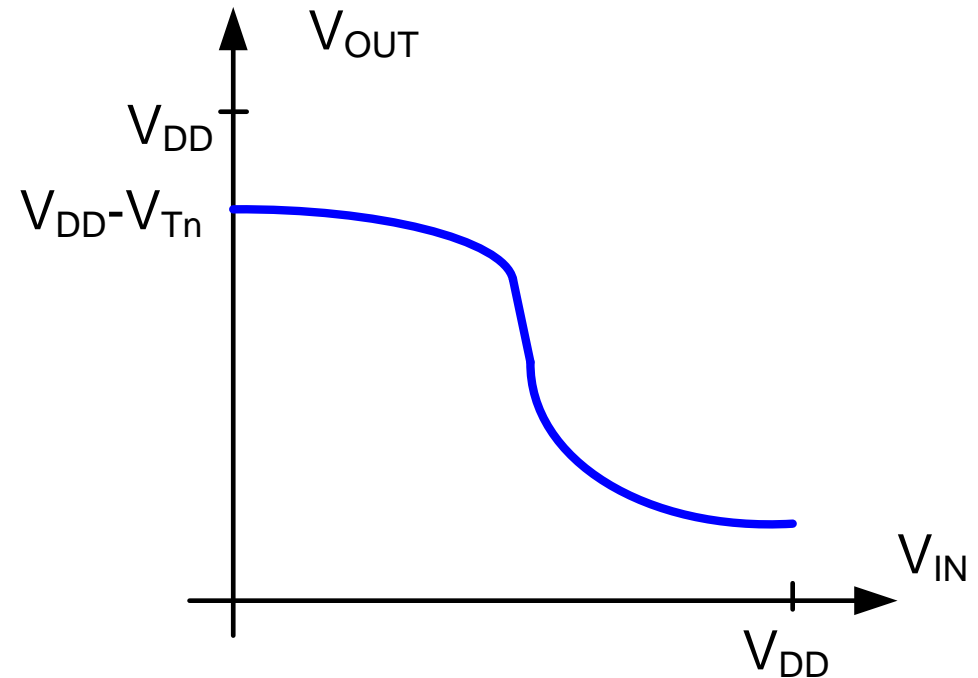
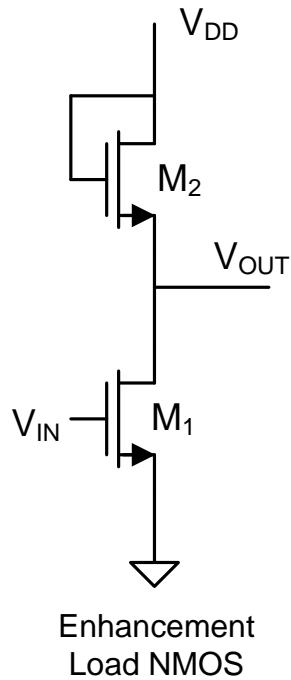


Enhancement Load
Pseudo-NMOS

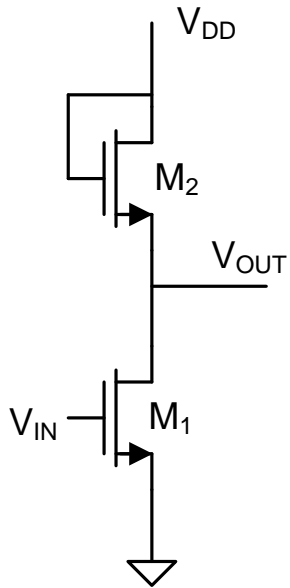


Depletion Load
NMOS

Other CMOS/MOS Logic Families



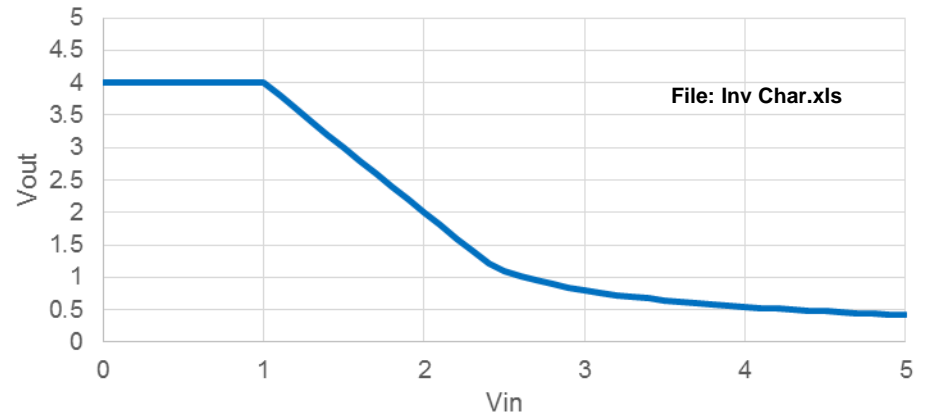
NMOS example



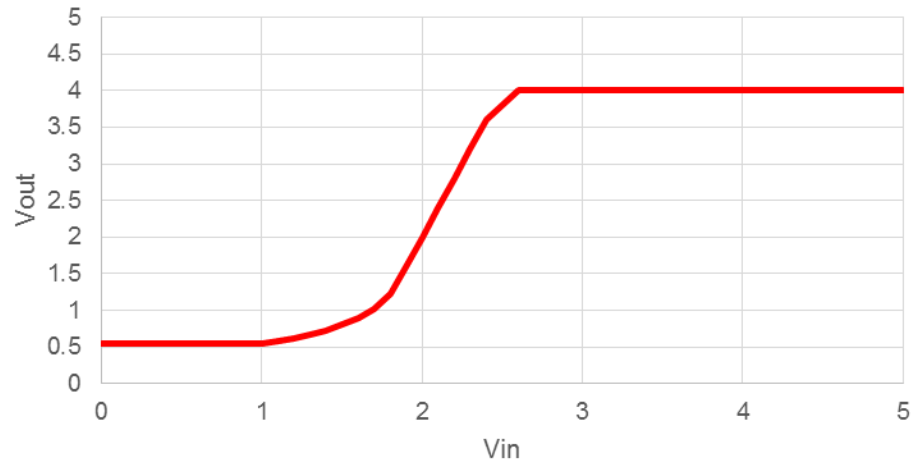
Enhancement
Load NMOS

V _{TH}		1
W ₁ /L ₁		4
W ₂ /L ₂		1
V _{DD}		5

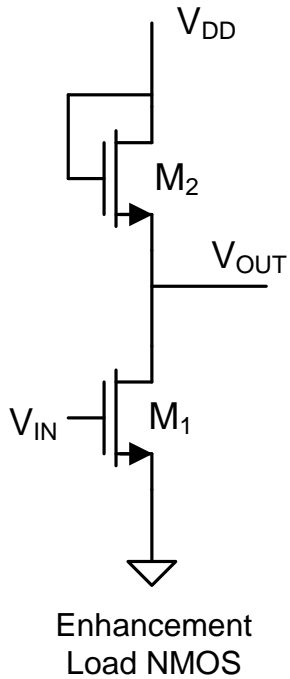
Inverter



Inverter Pair

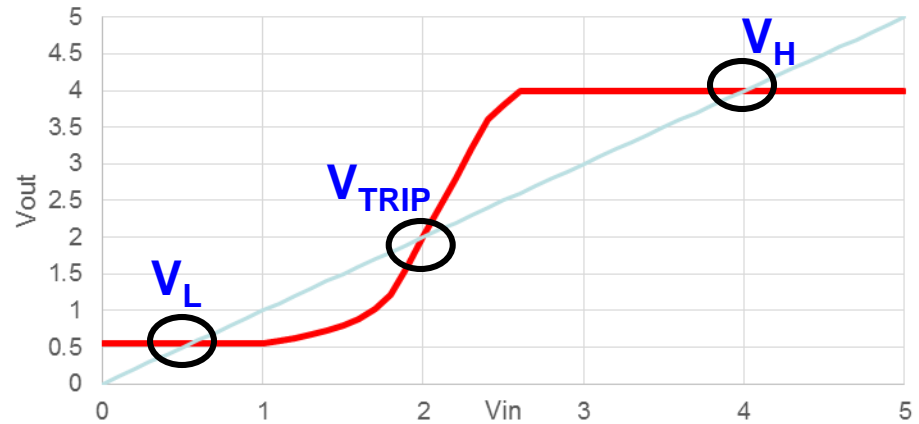


NMOS example



V _{TH}	1
W ₁ /L ₁	4
W ₂ /L ₂	1
V _{DD}	5

Inverter Pair

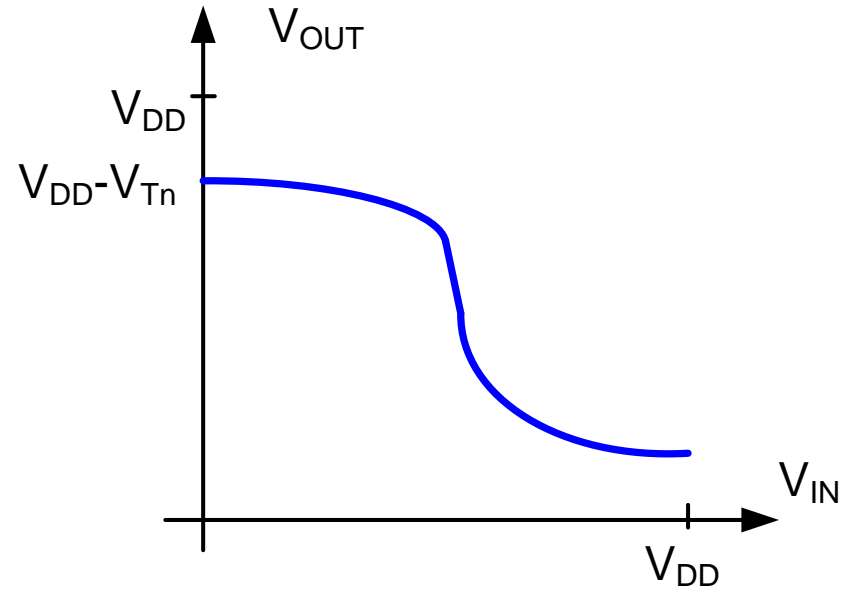
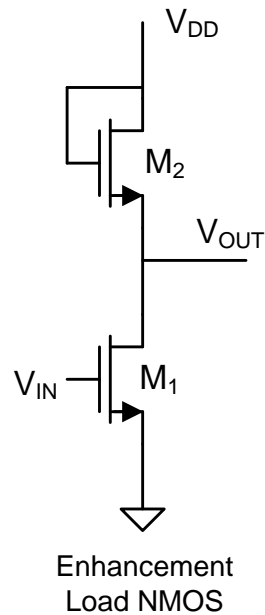







$$V_H = 4V$$

$$V_L = 0.55V$$

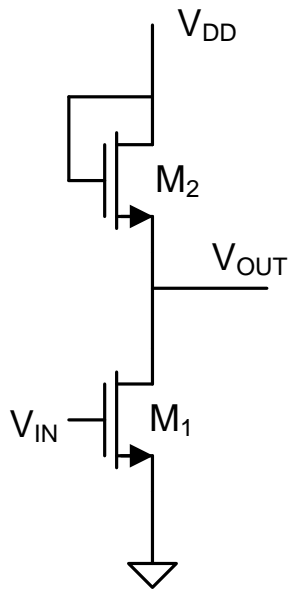
$$V_{TRIP} = 2V$$

Other CMOS/MOS Logic Families

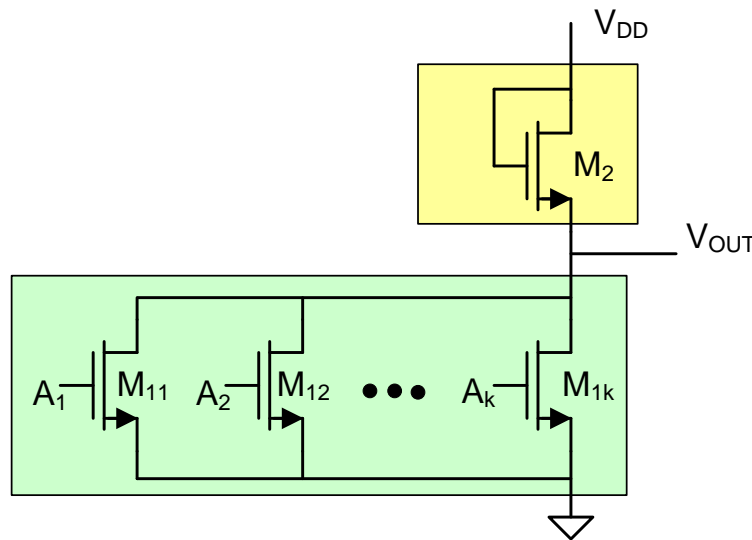


- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when V_{OUT} is low (will sl )
- Very economical process 
- Termed “ratio logic” (because logic values dependent on device W/L ratios – USE UP DOF!)
- May not work for some device sizes 
- Compact layout (no wells !)
- Can use very low cost process 
- Available to use in standard CMOS process 

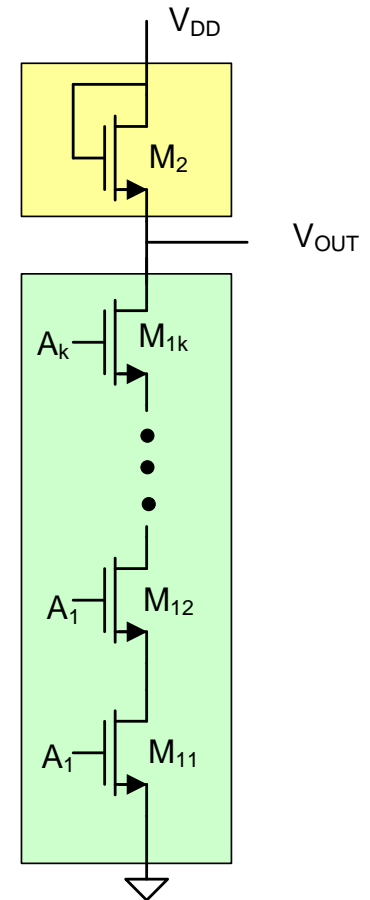
Other CMOS/MOS Logic Families



Enhancement
Load NMOS



k-input NOR



k-input NAND

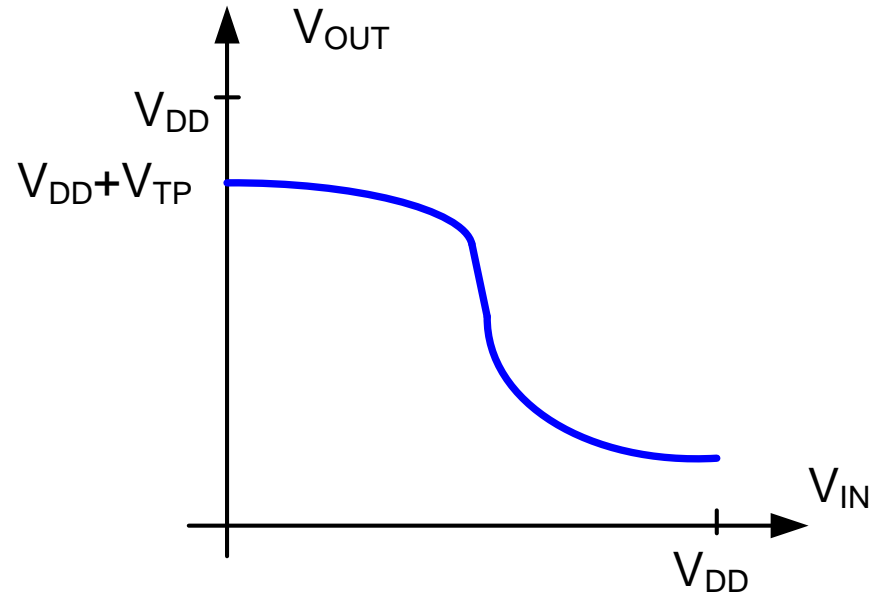
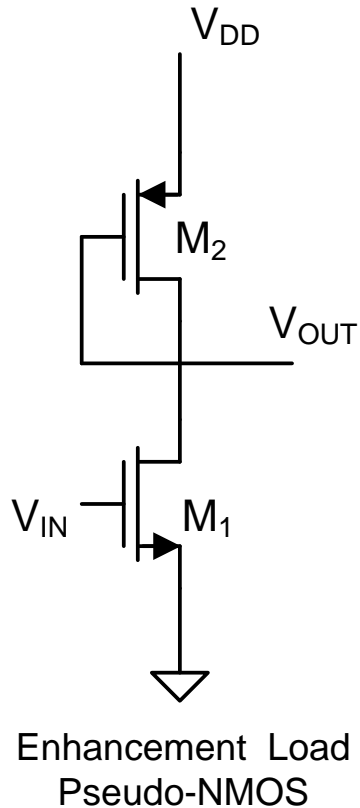
- **Multiple-input gates require single transistor for each additional input**



- **Still useful if many inputs are required**
(will be shown that static power does not increase with k)



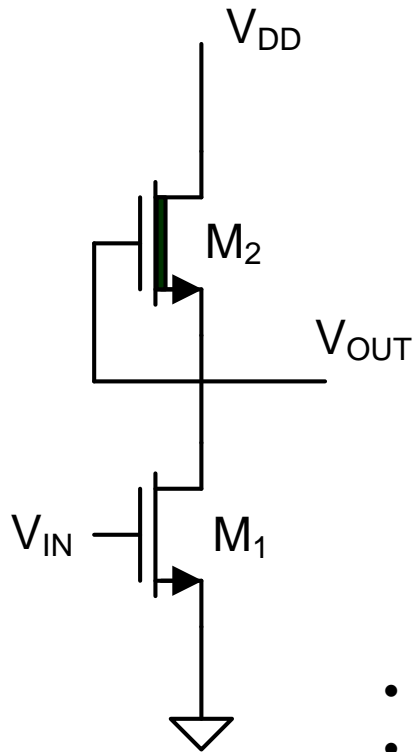
Other CMOS/MOS Logic Families



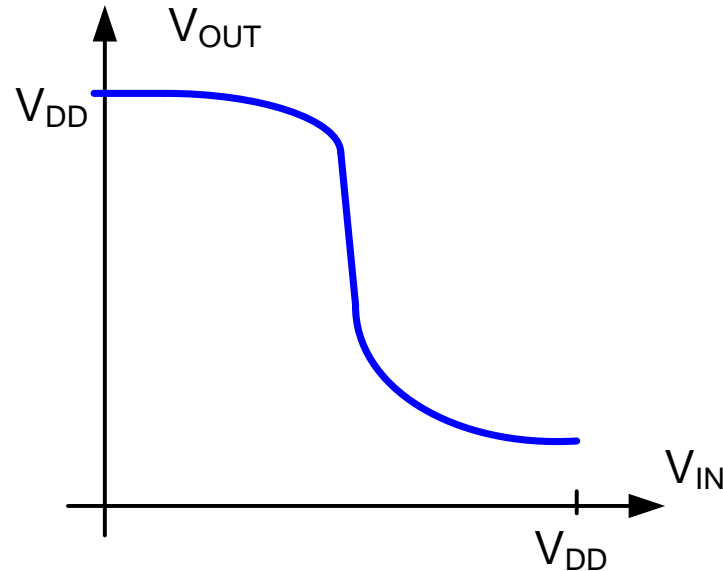
- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when V_{OUT} is low
- Multiple-input gates require single transistor for each additional input
- Termed “ratio” logic
- Available to use in standard CMOS process









Other CMOS/MOS Logic Families



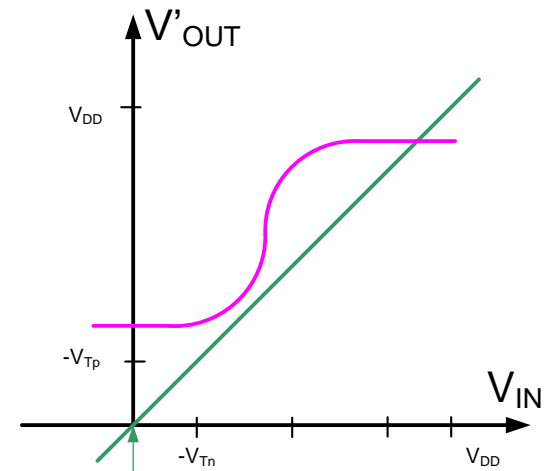
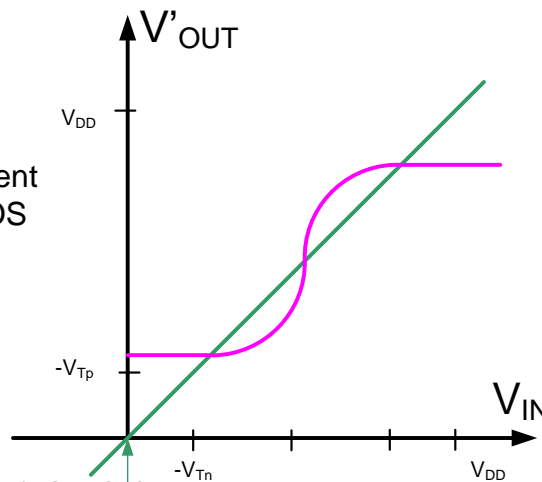
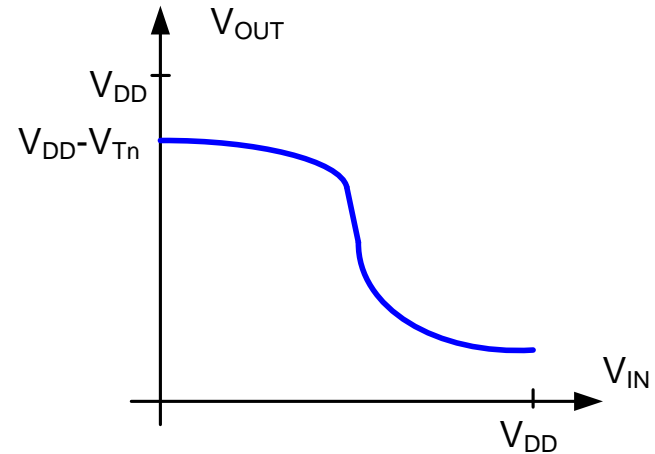
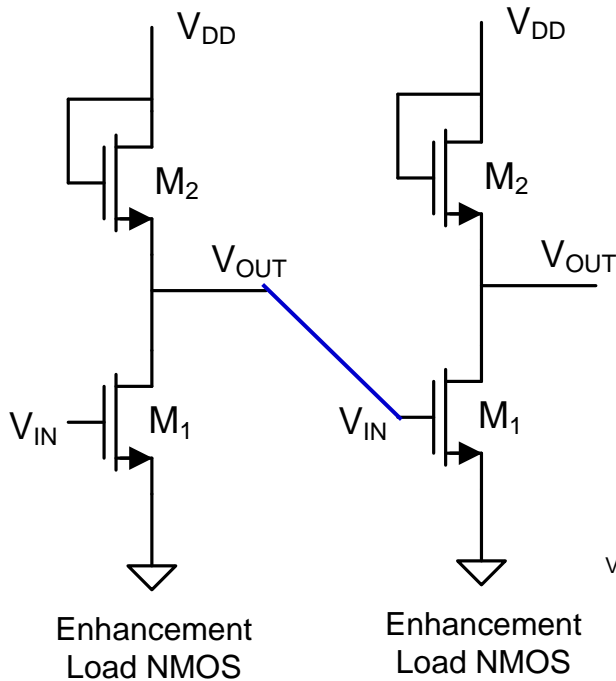
$$V_{TD} < 0$$



Depletion
Load NMOS

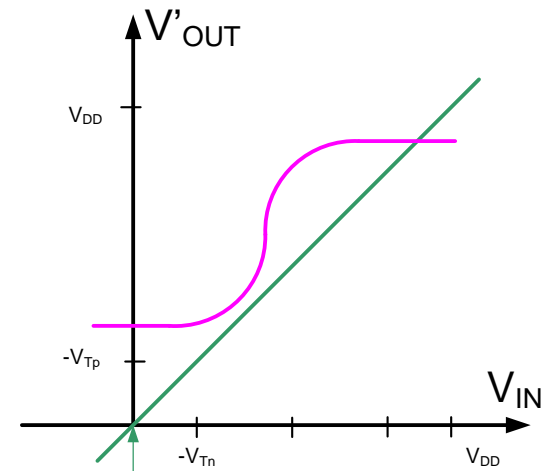
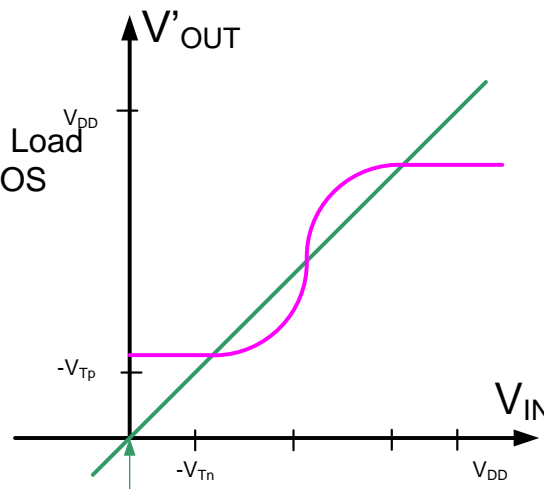
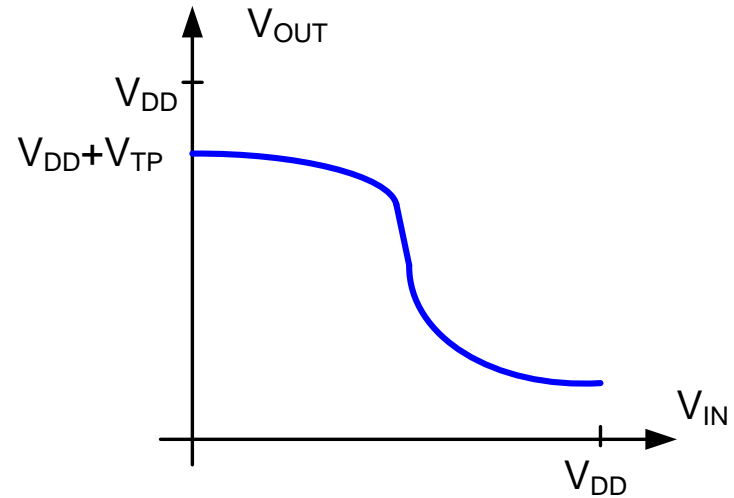
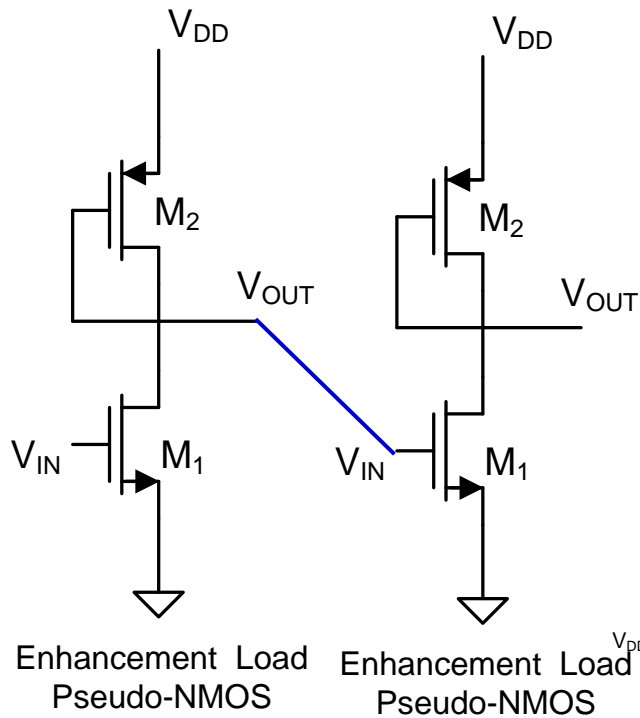
- Low swing is degraded 
- Static Power Dissipation Large when V_{OUT} is low 
- Very economical process 
- Better than Enhancement Load NMOS
- Termed “ratio” logic
- Compact layout (no wells !) 
- Slow on L-H output transitions (but not as slow as previous  ic)
- Dominant MOS logic until about 1985
- Depletion device not available in most processes today 

Other CMOS/MOS Logic Families



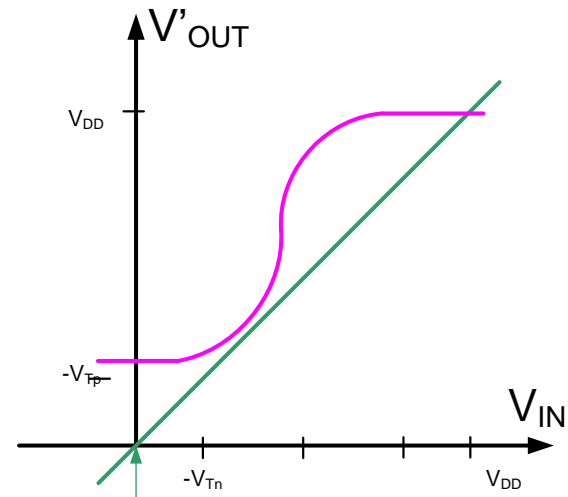
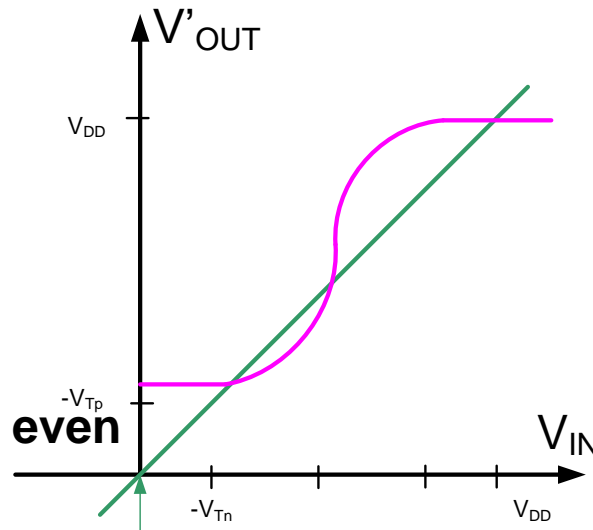
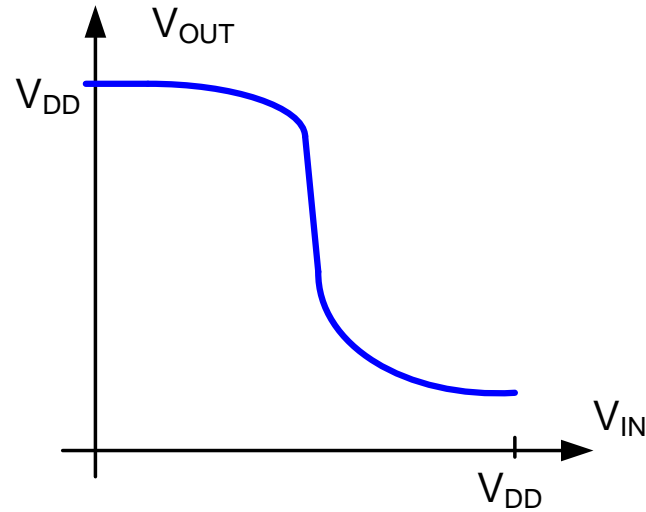
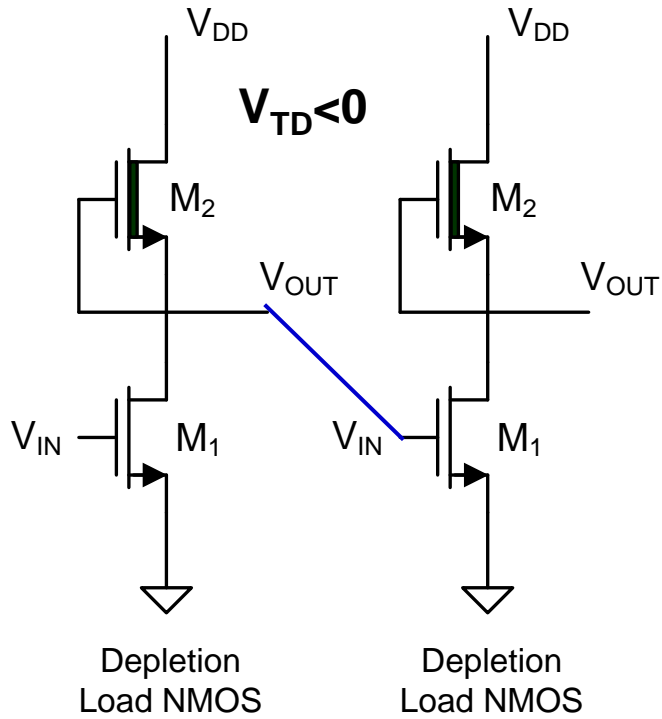
- **Reduced $V_H - V_L$**
- **Device sizing critical for even basic operation**
- **Shallow slope at V_{TRIP}**

Other CMOS/MOS Logic Families



- **Reduced $V_H - V_L$**
- **Device sizing critical for even basic operation (DOF)**
- **Shallow slope at V_{TRIP}**

Other CMOS/MOS Logic Families



- **Reduced $V_H - V_L$**
- **Device sizing critical for even basic operation**
- **Shallow slope at V_{TRIP}**

Digital Circuit Design

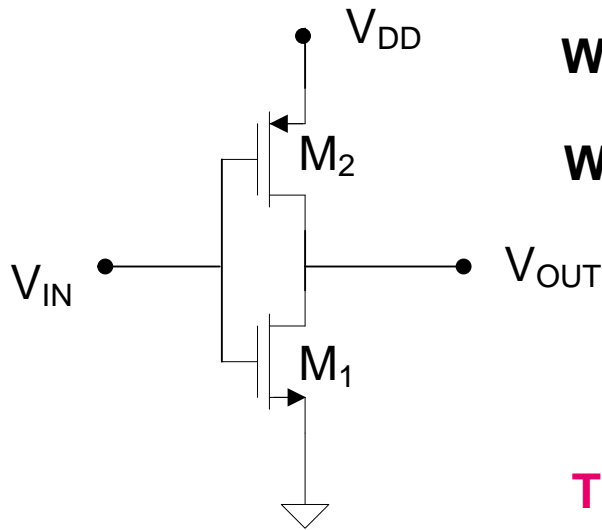
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→ **done**

→ **partial**

Static Power Dissipation in Static CMOS Family

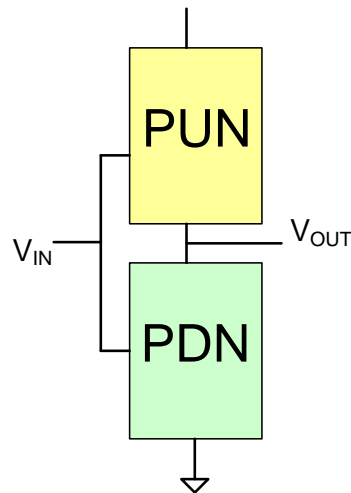


When V_{IN} is Low and V_{OUT} is High, M_1 is off and $I_{D1}=0$

When V_{IN} is High and V_{OUT} is Low, M_2 is off and $I_{D2}=0$

Thus, $P_{STATIC}=0$

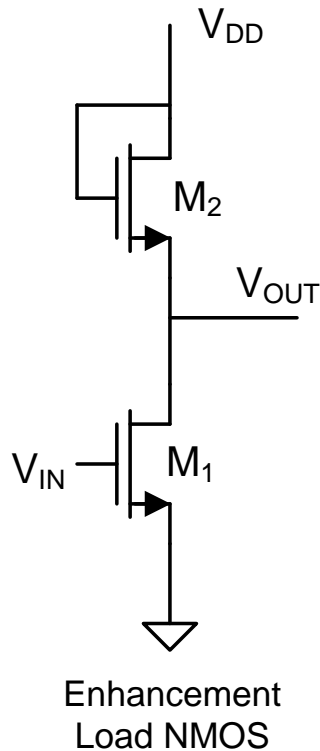
This is a key property of the static CMOS Logic Family → the major reason Static CMOS Logic is so dominant



It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of p-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time

Static Power Dissipation in Ratio Logic Families

Example:



Assume $V_{DD}=5V$

$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and M_2 sized so that V_L is close to V_{Tn}

Observe:

$$V_H=V_{DD}-V_{Tn}$$

If $V_{IN}=V_H$, $V_{OUT}=V_L$ so

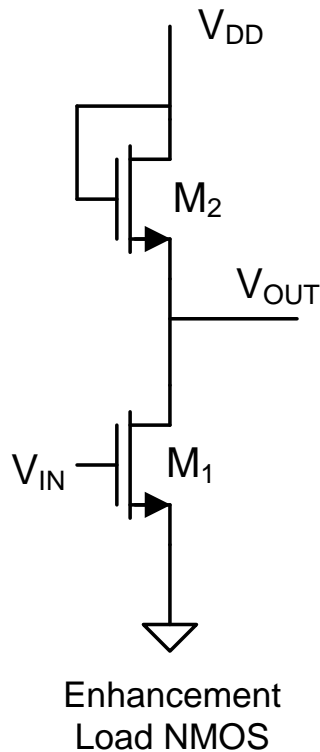
$$I_{D1} = \frac{\mu C_{OX} W_1}{L_1} \left(V_{GS1} - V_T - \frac{V_{DS1}}{2} \right) V_{DS1}$$

$$I_{D1} = 10^{-4} \left(5 - 1 - 1 - \frac{1}{2} \right) \cdot 1 = 0.25mA$$

$$P_L=(5V)(0.25mA)=1.25mW$$

Static Power Dissipation in Ratio Logic Families

Example:



Assume $V_{DD}=5V$

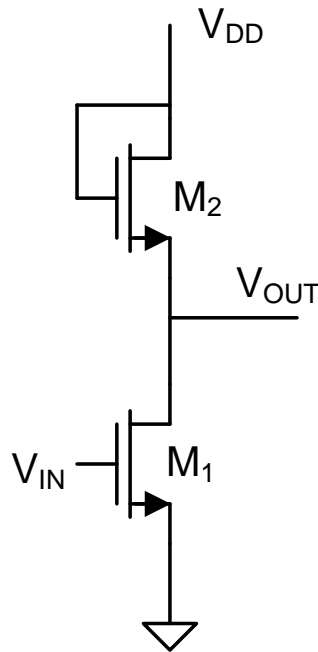
$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and M_2 sized so that V_L is close to V_{Tn}

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be

Static Power Dissipation in Ratio Logic Families

Example:



Enhancement
Load NMOS

Assume $V_{DD}=5V$

$V_T=1V$, $\mu C_{OX}=10^{-4}A/V^2$, $W_1/L_1=1$ and M_2 sized so that V_L is close to V_{Tn}

$$P_L=(5V)(0.25mA)=1.25mW$$

If a circuit has 100,000 gates and half of them are in the $V_{OUT}=V_L$ state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2} 10^5 \cdot 1.25mW = \mathbf{62.5W}$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today

Digital Circuit Design

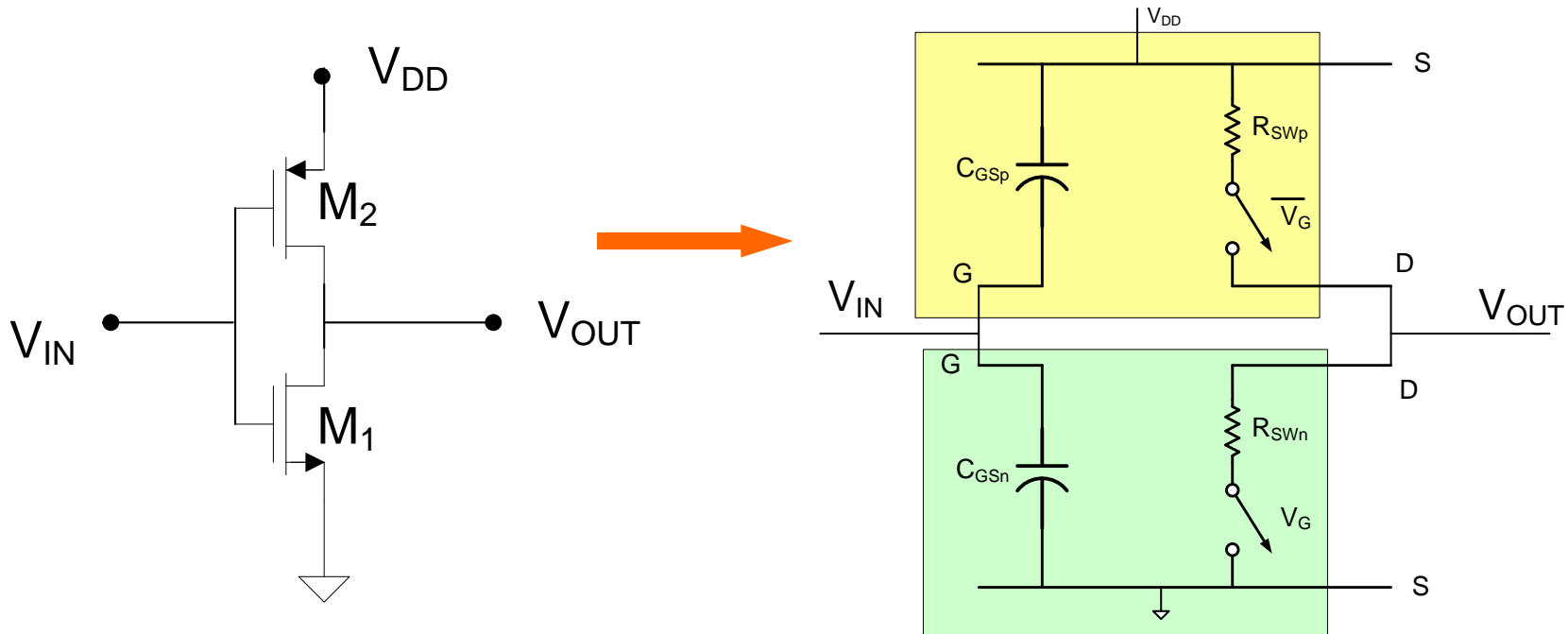
- Hierarchical Design
 - Basic Logic Gates
 - Properties of Logic Families
 - Characterization of CMOS Inverter
 - Static CMOS Logic Gates
 - Ratio Logic
 - Propagation Delay
 - Simple analytical models
 - FI/OD
 - Logical Effort
 - Elmore Delay
 - Sizing of Gates
 - The Reference Inverter
- Propagation Delay with Multiple Levels of Logic
 - Optimal driving of Large Capacitive Loads
 - Power Dissipation in Logic Circuits
 - Other Logic Styles
 - Array Logic
 - Ring Oscillators

→ **done**

→ **partial**

Propagation Delay in Static CMOS Family

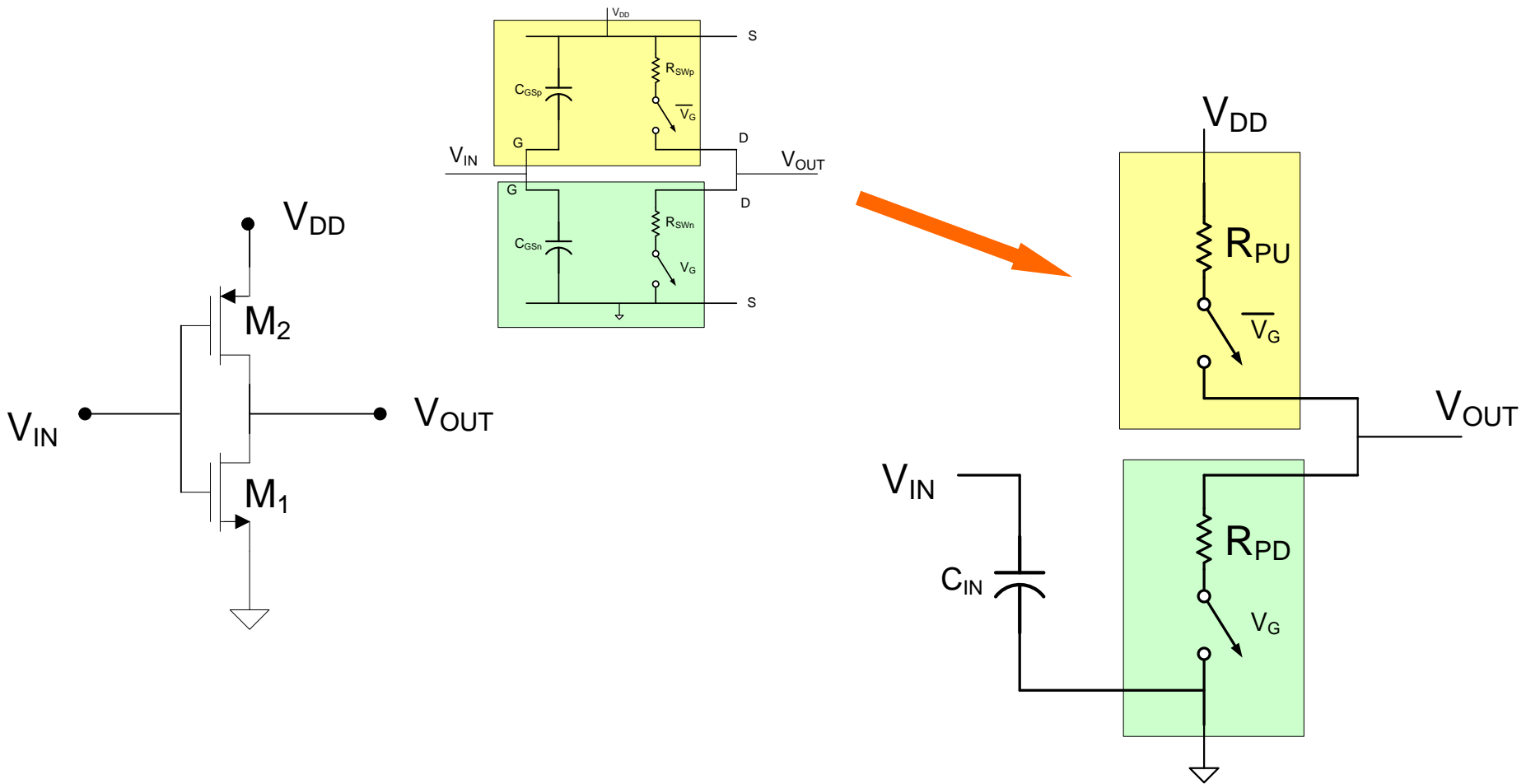
(Review from earlier discussions)



Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family

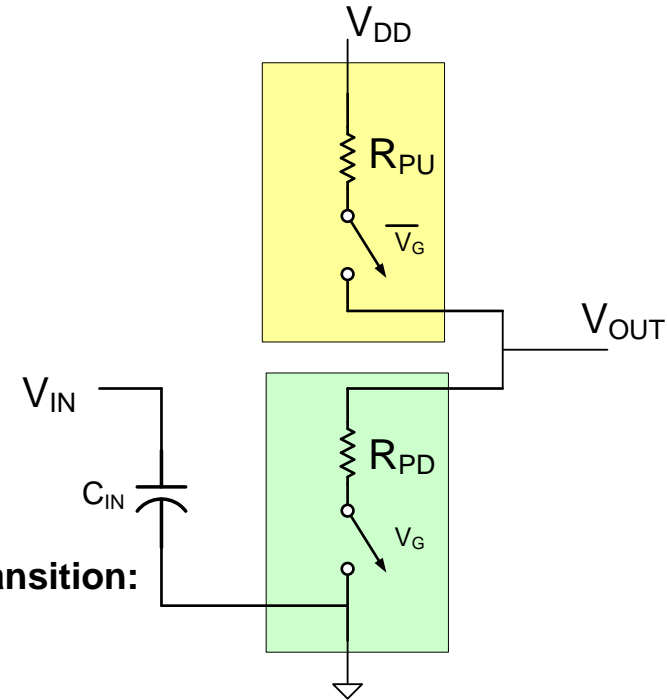
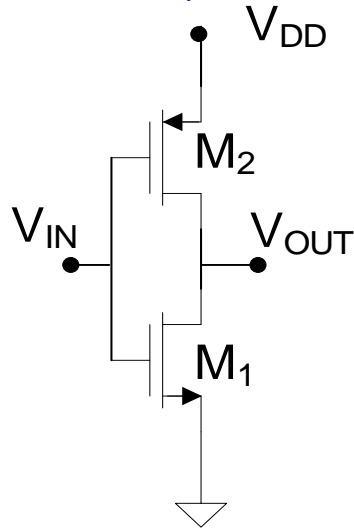
(Review from earlier discussions)



Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family

(Review from earlier discussions)



Since conducting transistor operating in triode through most of transition:

$$I_D \cong \frac{\mu C_{OX} W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \cong \frac{\mu C_{OX} W}{L} (V_{GS} - V_T) V_{DS}$$

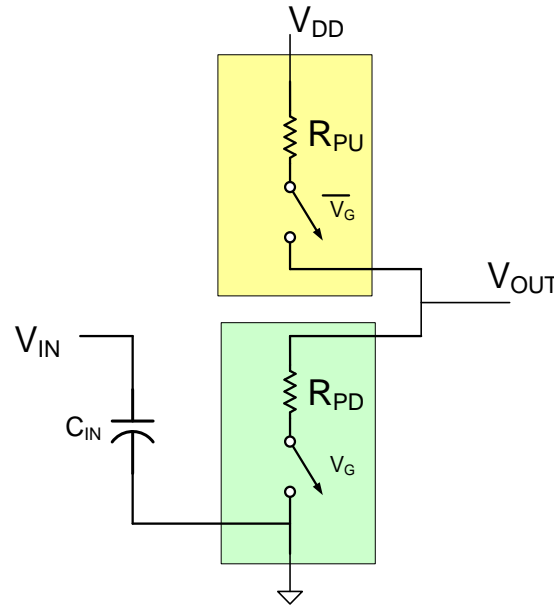
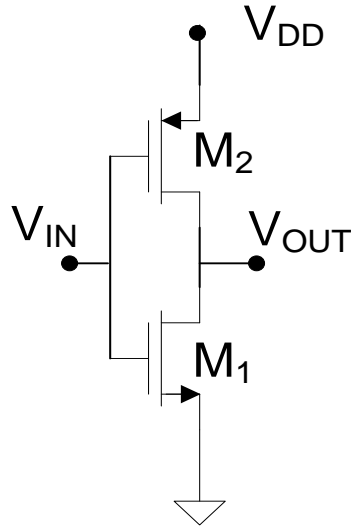
$$R_{PD} = \frac{V_{DS}}{I_D} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{V_{DS}}{I_D} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2)$$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)



$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2)$$

Example: Minimum-sized M_1 and M_2

If $\mu_n C_{OX} = 100 \mu A V^{-2}$, $C_{OX} = 4 \text{ fF} \mu^{-2}$, $V_{Tn} = V_{DD}/5$, $V_{Tp} = -V_{DD}/5$, $\mu_n/\mu_p = 3$, $L_1 = W_1 = L_{MIN}$, $L_2 = W_2 = L_{MIN}$, $L_{MIN} = 0.5 \mu$ and $V_{DD} = 5V$

(Note: This C_{ox} is somewhat larger than that in the 0.5u ON process)

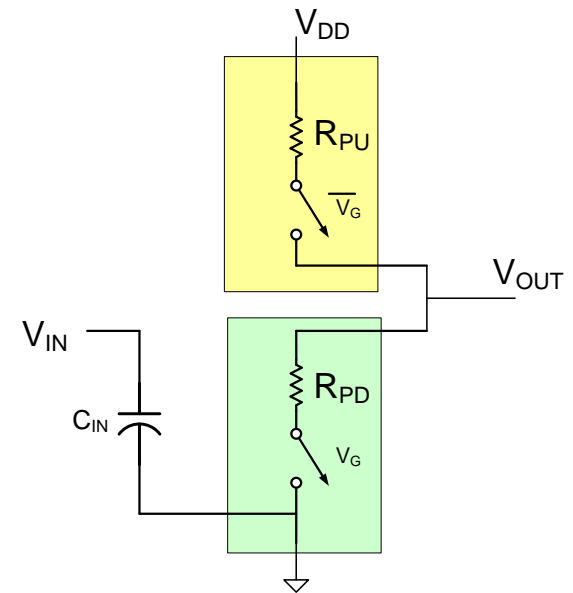
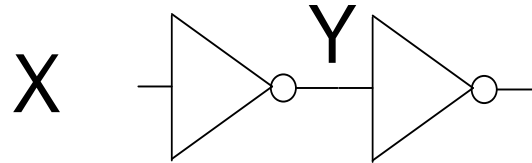
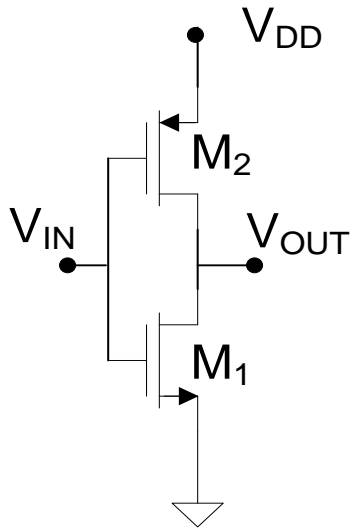
$$R_{PD} = \frac{1}{10^{-4} \cdot 0.8 V_{DD}} = 2.5 K\Omega$$

$$C_{IN} = 4 \cdot 10^{-15} \cdot 2 L_{MIN}^2 = 2 \text{ fF}$$

$$R_{PU} = \frac{1}{10^{-4} \cdot \frac{1}{3} \cdot 0.8 V_{DD}} = 7.5 K\Omega$$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)



In typical process with **Minimum-sized M_1 and M_2** :

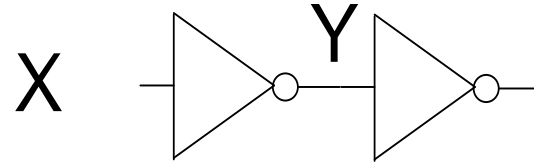
$$R_{PD} \cong 2.5K\Omega$$

$$R_{PU} \cong 3R_{PD} = 7.5K\Omega$$

$$C_{IN} \cong 2fF$$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)

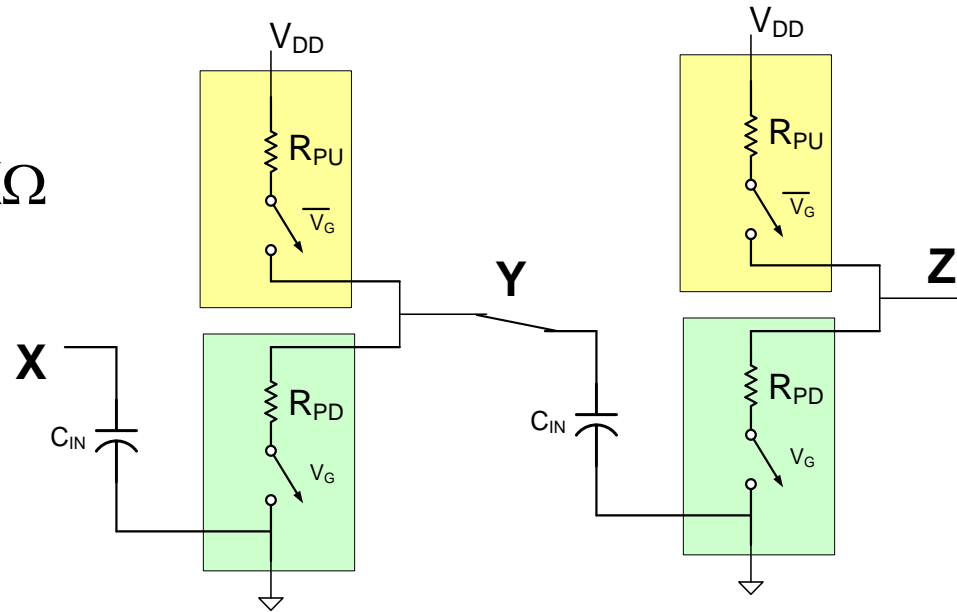


In typical process with **Minimum-sized M_1 and M_2** :

$$R_{PD} \cong 2.5K\Omega$$

$$R_{PU} \cong 3R_{PD} = 7.5K\Omega$$

$$C_{IN} \cong 2fF$$



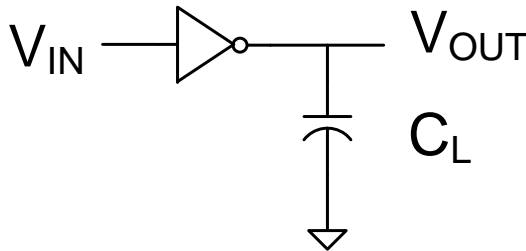
How long does it take for a signal to propagate from x to y?

Propagation Delay in Static CMOS Family

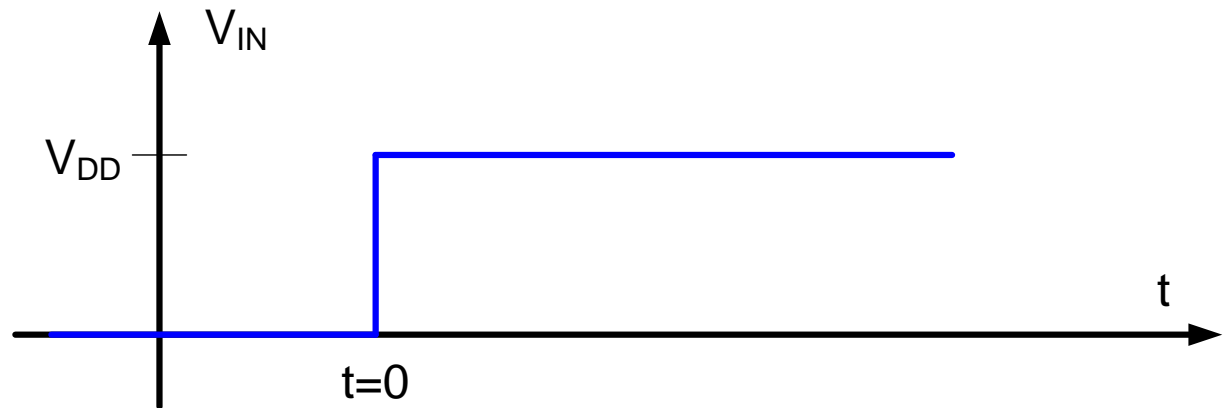
(Review from earlier discussions)

Consider:

For HL output transition, C_L charged to V_{DD}



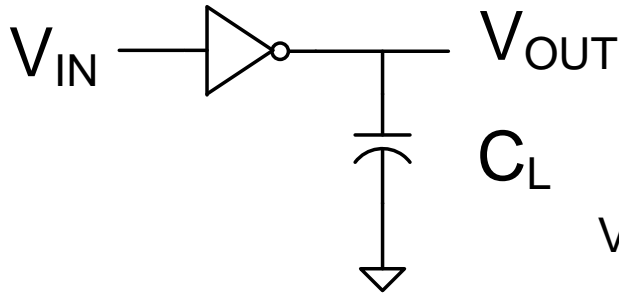
Ideally:



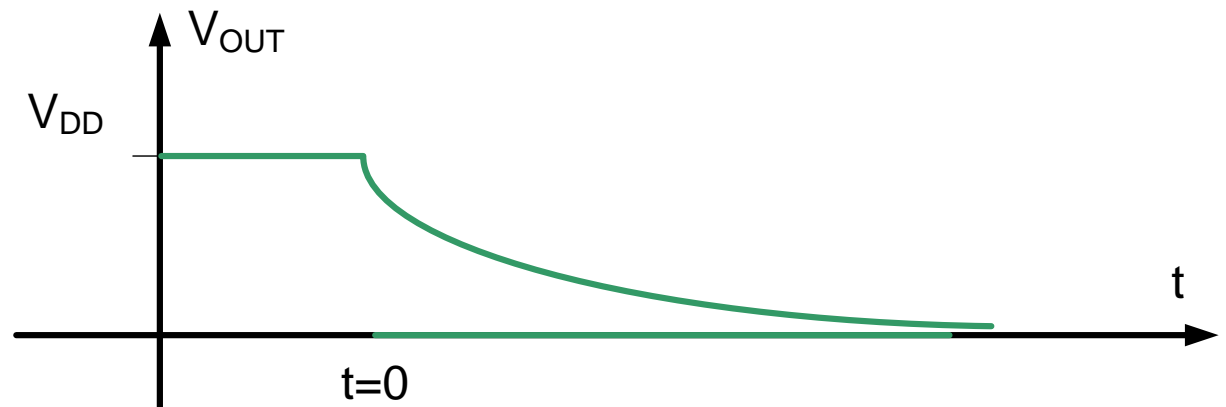
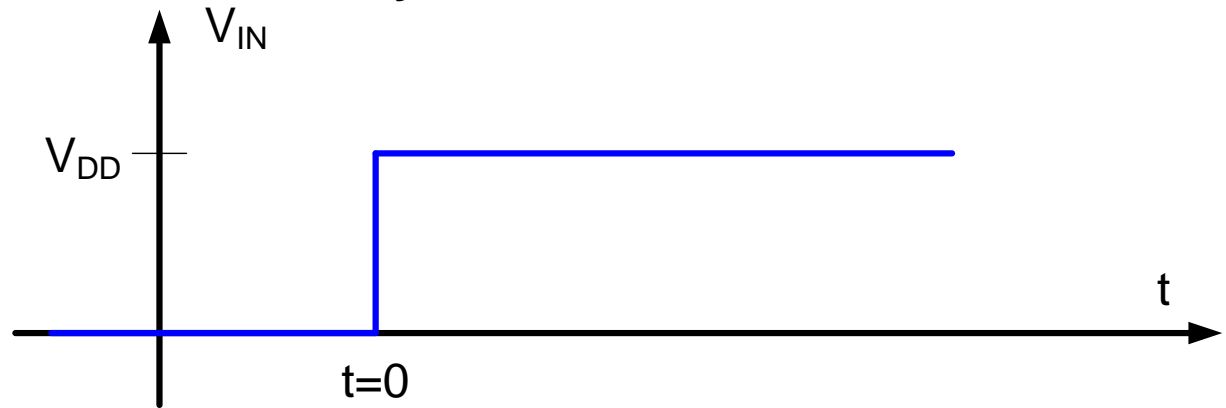
Propagation Delay in Static CMOS Family

(Review from earlier discussions)

For HL output transition, C_L charged to V_{DD}



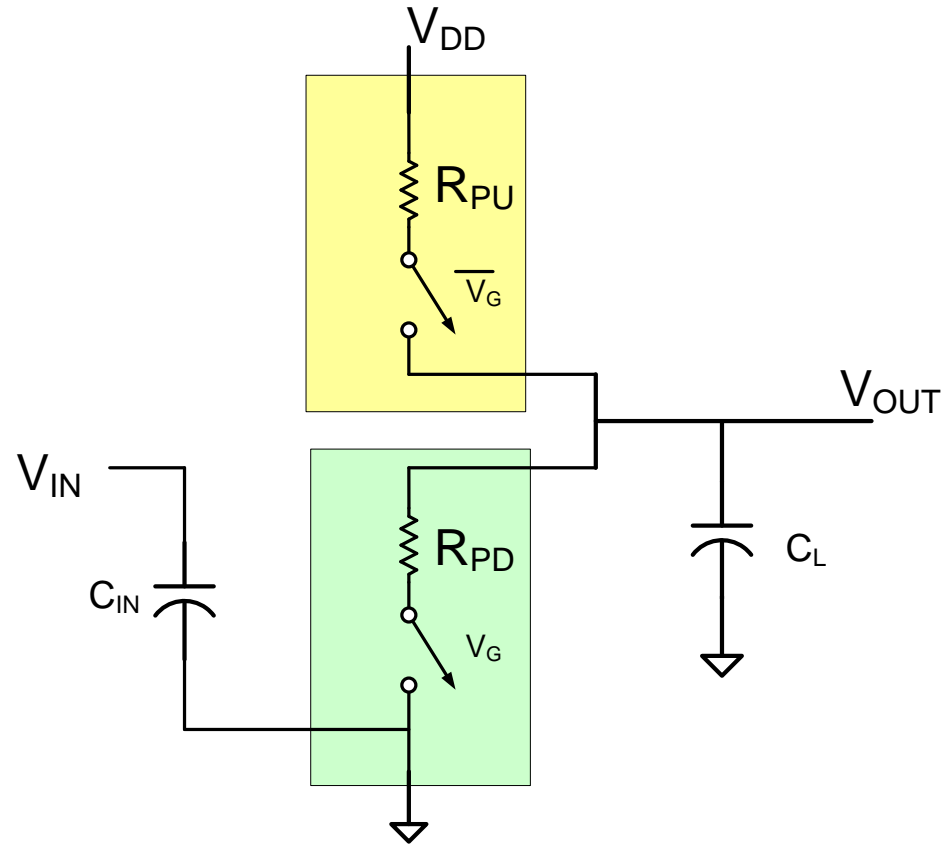
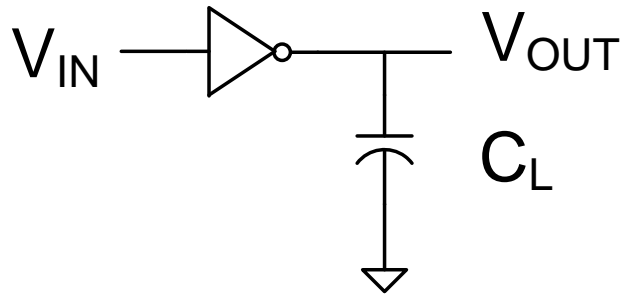
Actually:



What is the transition time t_{HL} ?

Propagation Delay in Static CMOS Family

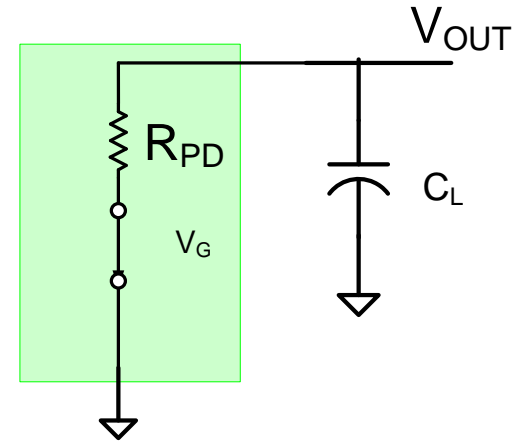
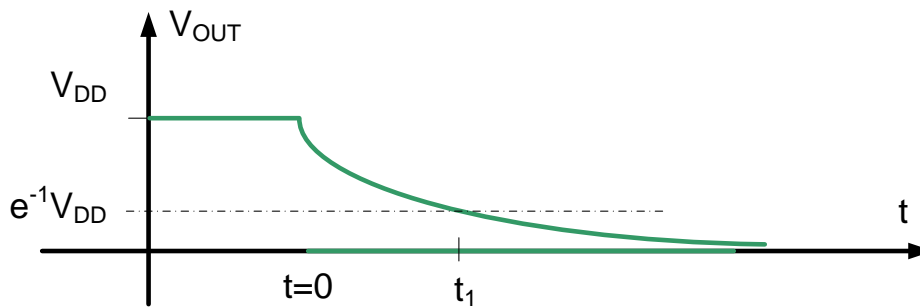
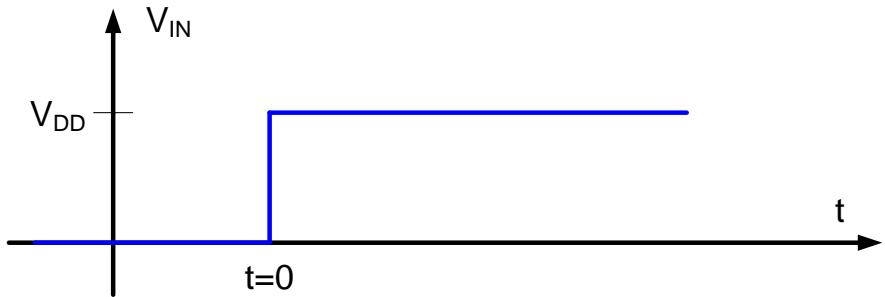
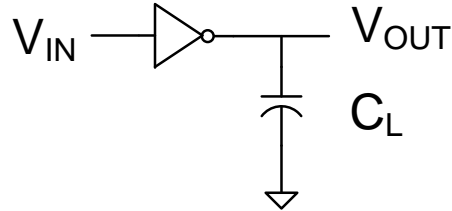
(Review from earlier discussions)



Propagation Delay in Static CMOS Family

(Review from earlier discussions)

For HL output transition, C_L charged to V_{DD}



$$V_{OUT}(t) = F + (I - F)e^{-\frac{t}{\tau}} = 0 + (V_{DD} - 0)e^{-\frac{t}{R_{PD}C_L}}$$

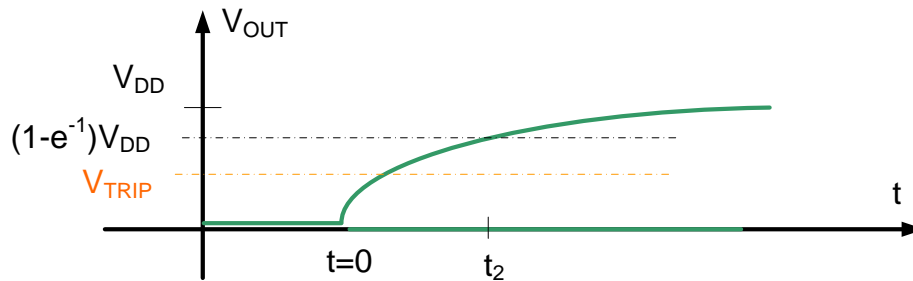
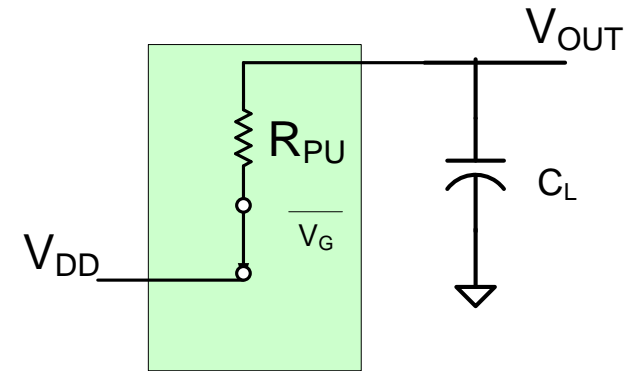
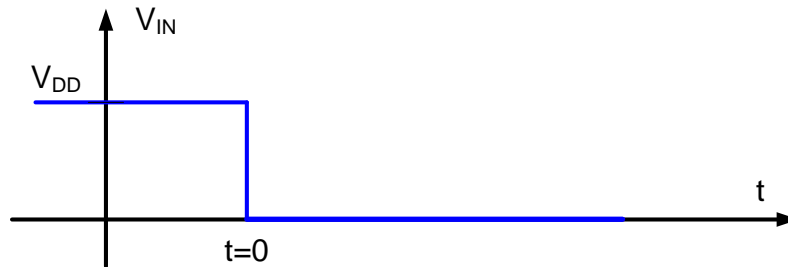
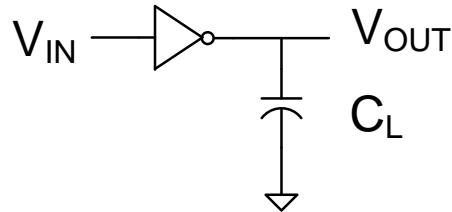
$$\frac{V_{DD}}{e} = V_{DD}e^{-\frac{t_1}{R_{PD}C_L}} \quad \longrightarrow \quad t_1 = R_{PD}C_L$$

If V_{TRIP} is close to $V_{DD}/2$, t_{HL} is close to t_1

Propagation Delay in Static CMOS Family

(Review from earlier discussions)

For HL output transition, C_L charged to V_{DD}



$$t_{LH} \cong t_2 = R_{PU} C_L$$

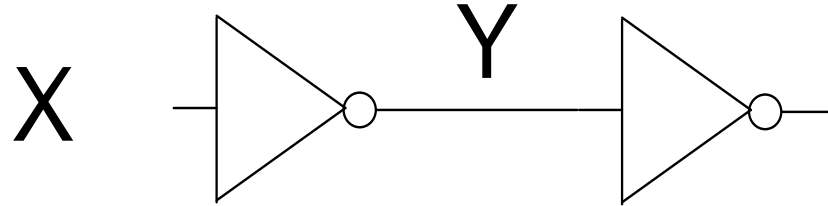
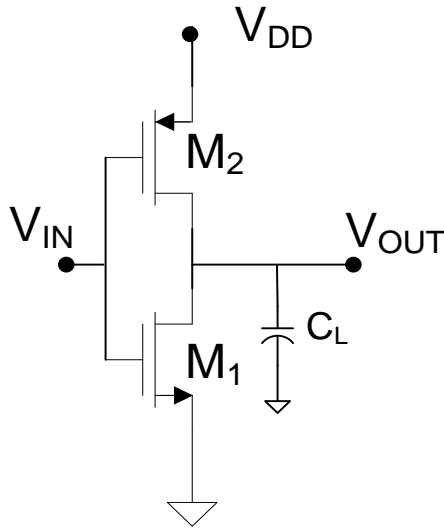
Summary: $t_{LH} \cong R_{PU} C_L$

$$t_{HL} \cong R_{PD} C_L$$

For V_{TRIP} close to $V_{DD}/2$

Propagation Delay in Static CMOS Family

(Review from earlier discussions)



In typical process with **Minimum-sized M_1 and M_2** :

$$t_{HL} \cong R_{PD}C_L \cong 2.5K \cdot 2fF = 5ps$$

$$t_{LH} \cong R_{PU}C_L \cong 7.5K \cdot 2fF = 15ps$$

(Note: This C_{ox} is somewhat larger than that in the 0.5u ON process)

Note: LH transition is much slower than HL transition

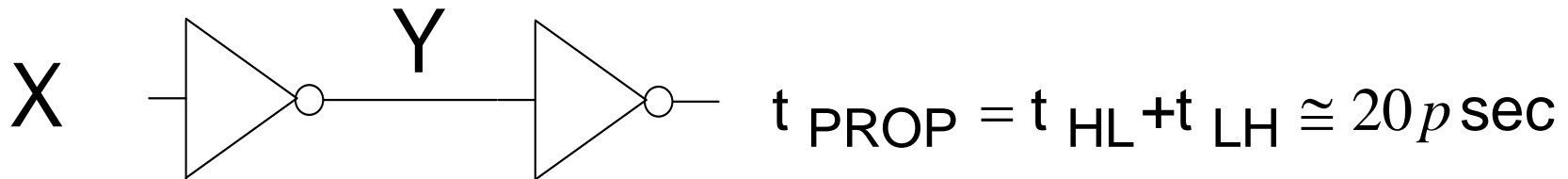
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of t_{HL} and t_{LH} , that is, $t_{PROP} = t_{HL} + t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L (R_{PU} + R_{PD})$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked at

For basic two-inverter cascade in static 0.5um CMOS logic driving an identical device



Propagation Delay in Static CMOS Family

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L (R_{PU} + R_{PD})$$

$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})} \quad R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})} \quad C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2)$$

If $V_{Tn} = -V_{Tp} = V_T$ and if $C_L = C_{IN}$

$$t_{PROP} = C_{OX} (W_1 L_1 + W_2 L_2) \left(\frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_T)} + \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} - V_T)} \right)$$

If $L_2 = L_1 = L_{min}$, $\mu_n = 3\mu_p$,

$$t_{PROP} = \frac{L_{min}^2}{\mu_n (V_{DD} - V_T)} (W_1 + W_2) \left(\frac{1}{W_1} + \frac{3}{W_2} \right) = \frac{L_{min}^2}{\mu_n (V_{DD} - V_T)} \left(4 + \frac{W_2}{W_1} + 3 \frac{W_1}{W_2} \right)$$

Note speed is a function of device sizing !

Can t_{PROP} be minimized?

Propagation Delay in Static CMOS Family

For $L_2 = L_1 = L_{\min}$, $\mu_n = 3\mu_p$,

$$t_{PROP} = \frac{L_{\min}^2}{\mu_n (V_{DD} - V_T)} \left(4 + \frac{W_2}{W_1} + 3 \frac{W_1}{W_2} \right)$$

Can t_{PROP} be minimized?

Assume $W_1 = W_{\min}$

$$\frac{\partial t_{PROP}}{\partial W_2} = \left[\frac{L_{\min}^2}{\mu_n (V_{DD} - V_{TH})} \right] \left[\frac{1}{W_{\min}} - 3 \frac{W_{\min}}{W_2^2} \right] = 0$$

$$\frac{1}{W_{\min}} - 3 \frac{W_{\min}}{W_2^2} = 0$$

$$W_2 = \sqrt{3} W_{\min}$$

$$t_{PROP} = \frac{L_{\min}^2}{\mu_n (V_{DD} - V_T)} (4 + 2\sqrt{3}) \cong \frac{L_{\min}^2}{\mu_n (V_{DD} - V_T)} (7.5) \quad (7.5)$$

Propagation Delay in Static CMOS Family

$$t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} \cong C_L (R_{\text{PU}} + R_{\text{PD}})$$

If $V_{\text{Tn}} = -V_{\text{Tp}} = V_{\text{T}}$ and $C_L = C_{\text{IN}}$

For min size:

$$t_{\text{PROP}} = C_{\text{OX}} (W_1 L_1 + W_2 L_2) \left(\frac{L_1}{\mu_n C_{\text{OX}} W_1 (V_{\text{DD}} - V_{\text{T}})} + \frac{L_2}{\mu_p C_{\text{OX}} W_2 (V_{\text{DD}} - V_{\text{T}})} \right)$$

If $L_2 = L_1 = L_{\text{min}}$, $W_1 = W_2 = W_{\text{min}}$, $\mu_n = 3\mu_p$,

$$t_{\text{PROP}} = \frac{L_{\text{min}}^2}{\mu_n (V_{\text{DD}} - V_{\text{T}})} (W_1 + W_2) \left(\frac{1}{W_1} + \frac{3}{W_2} \right) = \frac{L_{\text{min}}^2}{\mu_n (V_{\text{DD}} - V_{\text{T}})} (2W_{\text{min}}) \left(\frac{1}{W_{\text{min}}} + \frac{3}{W_{\text{min}}} \right)$$

For min size:

$$W_2 = W_1 = W_{\text{min}}$$

$$t_{\text{PROP}} = \frac{8L_{\text{min}}^2}{\mu_n (V_{\text{DD}} - V_{\text{T}})}$$

Propagation Delay in Static CMOS Family

$$t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} \cong C_L (R_{\text{PU}} + R_{\text{PD}})$$

If $V_{\text{Tn}} = -V_{\text{Tp}} = V_{\text{T}}$ and $C_L = C_{\text{IN}}$

For equal rise/fall:

$$t_{\text{PROP}} = C_{\text{OX}} (W_1 L_1 + W_2 L_2) \left(\frac{L_1}{\mu_n C_{\text{OX}} W_1 (V_{\text{DD}} - V_{\text{T}})} + \frac{L_2}{\mu_p C_{\text{OX}} W_2 (V_{\text{DD}} - V_{\text{T}})} \right)$$

If $L_2 = L_1 = L_{\text{min}}$, $W_1 = W_{\text{min}}$, $\mu_n = 3\mu_p$,

$$t_{\text{PROP}} = \frac{L_{\text{min}}^2}{\mu_n (V_{\text{DD}} - V_{\text{T}})} (W_1 + W_2) \left(\frac{1}{W_1} + \frac{3}{W_2} \right) \quad \longrightarrow \quad W_2 = 3W_1$$

For equal rise/fall:

$$W_2 = 3W_1$$

$$t_{\text{PROP}} = \frac{8L_{\text{min}}^2}{\mu_n (V_{\text{DD}} - V_{\text{T}})}$$

Propagation Delay in Static CMOS Family

$$t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} \cong C_L (R_{\text{PU}} + R_{\text{PD}})$$

Summary:

If $V_{\text{Tn}} = -V_{\text{Tp}} = V_{\text{T}}$ and $C_L = C_{\text{IN}}$ and $L_2 = L_1 = L_{\text{min}}$, $\mu_n = 3\mu_p$,

For min size:

$$W_2 = W_1 = W_{\text{min}}$$

$$t_{\text{PROP}} = \frac{8L_{\text{min}}^2}{\mu_n (V_{\text{DD}} - V_{\text{T}})}$$

For equal rise/fall:

$$W_2 = 3W_1$$

$$t_{\text{PROP}} = \frac{8L_{\text{min}}^2}{\mu_n (V_{\text{DD}} - V_{\text{T}})}$$

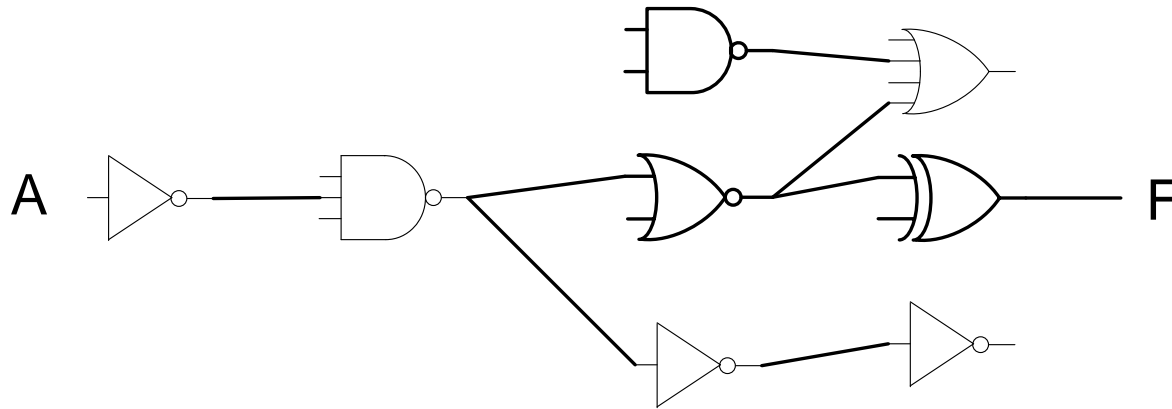
For min delay:

$$W_2 = \sqrt{3}W_1$$

$$t_{\text{PROP}} = \frac{(4 + 2\sqrt{3})L_{\text{min}}^2}{\mu_n (V_{\text{DD}} - V_{\text{T}})} \quad (4 + 2\sqrt{3}) \cong 7.5$$

Propagation Delay About the Same for 3 Sizing Strategies

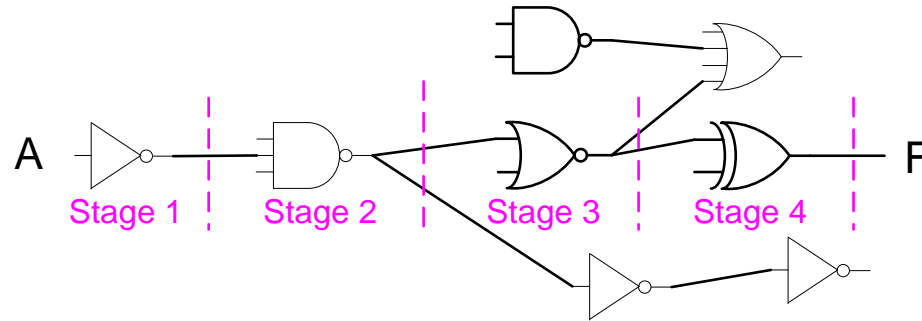
Propagation Delay in Static CMOS Family



The propagation delay through k levels of logic is approximately the sum of the individual propagation delays in the same path

Propagation Delay in Static CMOS Family

Example:



$$t_{HL} = t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1}$$

$$t_{LH} = t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1}$$

$$t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL3} + t_{LH2} + t_{HL1}) + (t_{HL4} + t_{LH3} + t_{HL2} + t_{LH1})$$

$$t_{PROP} = t_{LH} + t_{HL} = (t_{LH4} + t_{HL4}) + (t_{LH3} + t_{HL3}) + (t_{LH2} + t_{HL2}) + (t_{LH1} + t_{HL1})$$

$$t_{PROP} = t_{PROP4} + t_{PROP3} + t_{PROP2} + t_{PROP1}$$



Stay Safe and Stay Healthy !

End of Lecture 39